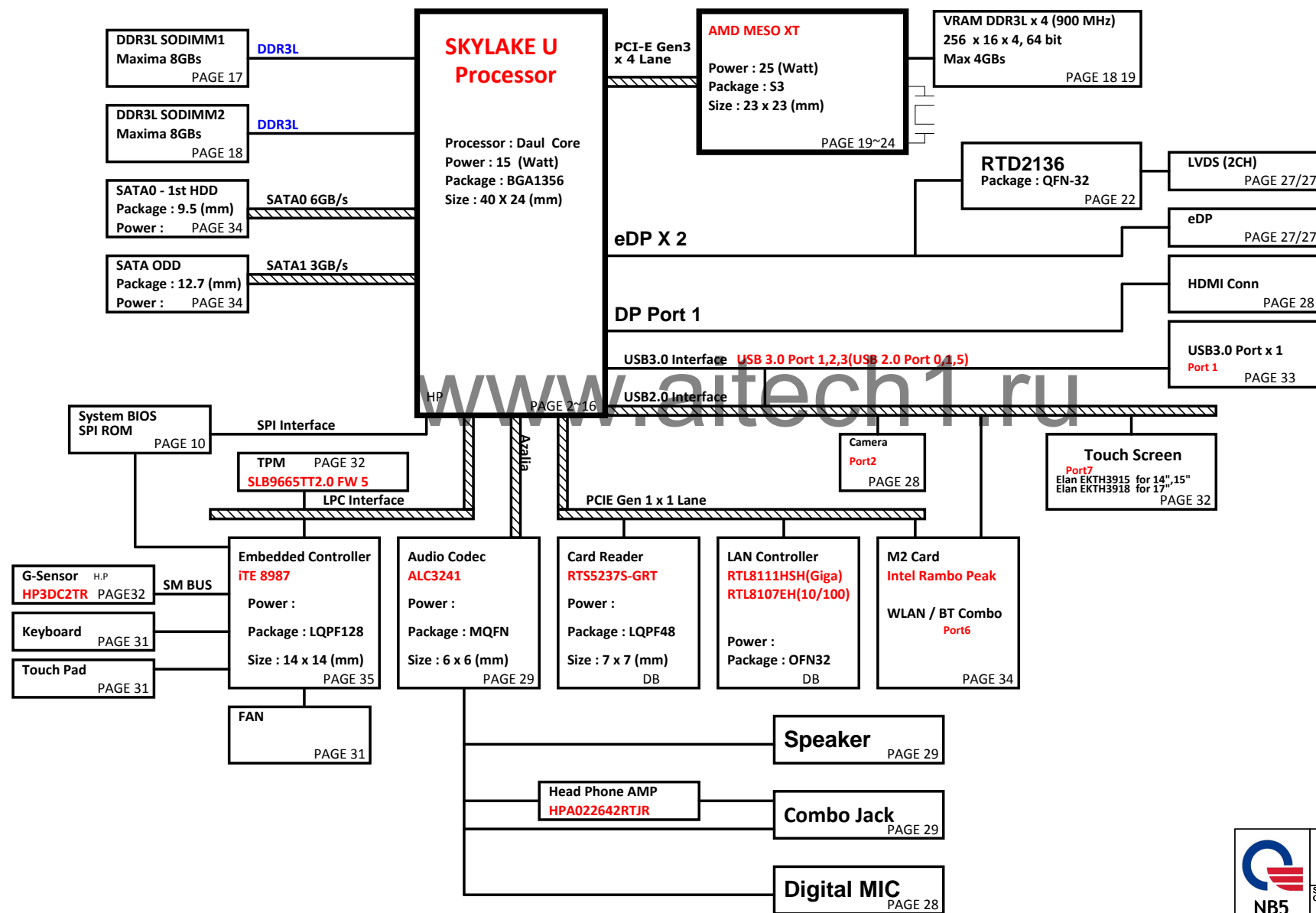


# Chocolate DIS (14" / 15" / 17") Intel SKYLAKE ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : BOT



+3V [4,10,11,12,13,14,15,16,17,18,27,28,29,30,31,32,33,34,35,41,43]  
 +1.0V [4,6,16,32,35,40]  
 +VCCSTPLL [4,5,6,9,40,41]  
 +VCCIO [6,16,40]

## HDMI

[28] IN\_D2# IN\_D2# E55  
 [28] IN\_D2 IN\_D2 F55  
 [28] IN\_D1# IN\_D1# F58  
 [28] IN\_D1 IN\_D1 F58  
 [28] IN\_D0# IN\_D0# G53  
 [28] IN\_D0 IN\_D0 G53  
 [28] IN\_CLK# IN\_CLK# F56  
 [28] IN\_CLK IN\_CLK G56

U17A

SKL\_ULI ?

Need apply PN

DDI1\_TXN[0] E55  
 DDI1\_TXP[0] F55  
 DDI1\_TXN[1] F58  
 DDI1\_TXP[1] F58  
 DDI1\_TXN[2] G53  
 DDI1\_TXP[2] G53  
 DDI1\_TXN[3] F56  
 DDI1\_TXP[3] F56  
 DDI2\_TXN[0] C50  
 DDI2\_TXP[0] C50  
 DDI2\_TXN[1] C52  
 DDI2\_TXP[1] C52  
 DDI2\_TXN[2] A53  
 DDI2\_TXP[2] A53  
 DDI2\_TXN[3] D51  
 DDI2\_TXP[3] D51

DISPLAY SIDEBANDS

[28] SDVO\_CLK  
 [28] SDVO\_DATA

TP121

DDPC\_CTRLDATA

TP122

DDPD\_CTRLDATA

+VCCIO

R96

24.9/F 4

EDP\_RCOMP

E52

eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms  
 1125 change R96 connection from +1.0V to +VCCIO

1222 del for DDP not use

EDP\_TXN[0] C47  
 EDP\_TXP[0] C46  
 EDP\_TXN[1] C46  
 EDP\_TXP[1] C45  
 EDP\_TXN[2] A45  
 EDP\_TXP[2] A45  
 EDP\_TXN[3] A47  
 EDP\_TXP[3] A47

INT\_EDP\_TXN0 [27]  
 INT\_EDP\_TXP0 [27]  
 INT\_EDP\_TXN1 [27]  
 INT\_EDP\_TXP1 [27]

INT\_EDP\_AUXN [27]  
 INT\_EDP\_AUXP [27]

EDP\_DISP\_UTIL B52  
 TP46

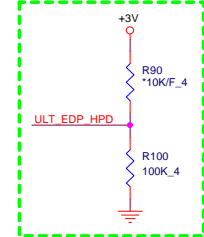
DDI1\_AUXN C50  
 DDI1\_AUXP C50  
 DDI2\_AUXN C48  
 DDI2\_AUXP C48  
 DDI3\_AUXN C46  
 DDI3\_AUXP C46

HDMI\_HPD\_CON L9  
 HDMI\_HPD\_CON [28]

ULT\_EDP\_HPD L10  
 ULT\_EDP\_HPD [27,28]

PCH\_LVDS\_BLON R12  
 PCH\_DPST\_PWM R11  
 PCH\_DISP\_ON U13

Reserve EDP\_HPD opposites circuit!



Need apply PN

U17D

SKL\_ULI ?

JTAG

CATER# D63  
 EC\_PECI A57  
 PROCHOT# C53  
 PM\_THRMTRIP# A55  
 SKT\_TCK# CPU#3  
 BPM#0 C55  
 BPM#1 B54  
 BPM#2 C56  
 BPM#3 C56

[33] 3D\_FW\_GPIO R557  
 0.4 3D\_FW\_GPIO\_R A6

TP98 CPU GP1 A7  
 TP98 CPU GP2 BA5  
 TP97 CPU GP3 AY5

R198 49.9/F 4 PROC\_POPIRCOMP AT16  
 R191 49.9/F 4 PCH\_OPI\_RCOMP AU16  
 R107 49.9/F 4 EDRAM\_OPIO\_RCOMP H66  
 R101 49.9/F 4 EOPIO\_RCOMP H65

XDP\_TCK0 [16]  
 XDP\_TDI\_CPU [16]  
 XDP\_TDO\_CPU [16]  
 XDP\_TMS\_CPU [16]  
 XDP\_TRST#\_CPU [2,16]

JTAG\_TCK\_PCH [16]  
 JTAG\_TDI\_PCH [16]  
 JTAG\_TDO\_PCH [16]  
 JTAG\_TMS\_PCH [16]  
 JTAGX\_PCH [16]

+VCCSTPLL R405  
 49.9/F 4 CATER#

+1.0V R74  
 0.4/S

0114  
 Del TP39, Add R557 with 0ohm mount for 3D camera

R389 51 4 JTAGX\_PCH  
 R390 51 4 JTAG\_TMS\_PCH  
 R407 51 4 JTAG\_TDI\_PCH  
 R408 51 4 JTAG\_TDO\_PCH  
 R391 51 4 JTAG\_TCK\_PCH

Close to Chipset

Close to EC

PM\_THRMTRIP# R404  
 1K 4

Processor pull-up (CPU)  
 TO BE REPLACED WITH 1K OHMS FOR SKL  
 470 OHM IS FOR I/P

PLACE NEAR CPU

XDP\_TMS\_CPU R392  
 51 4  
 XDP\_TDI\_CPU R388  
 51 4  
 XDP\_TDO\_CPU R378  
 51 4

1231 un-install R378, R392

H\_PROCHOT# R44  
 1K 4

XDP\_TCK0 R406  
 51 4  
 XDP\_TRST#\_CPU R384  
 51 4



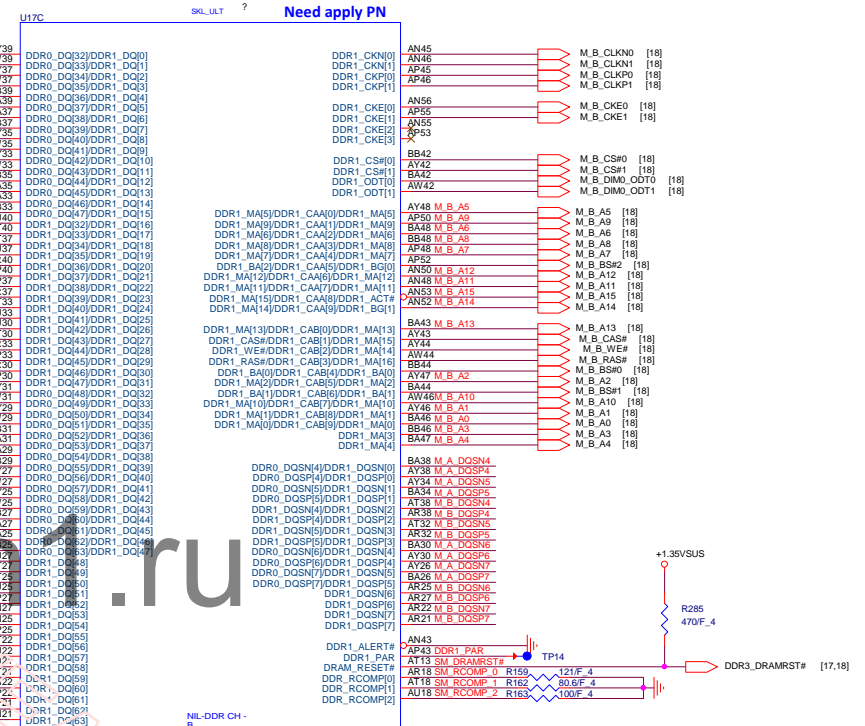
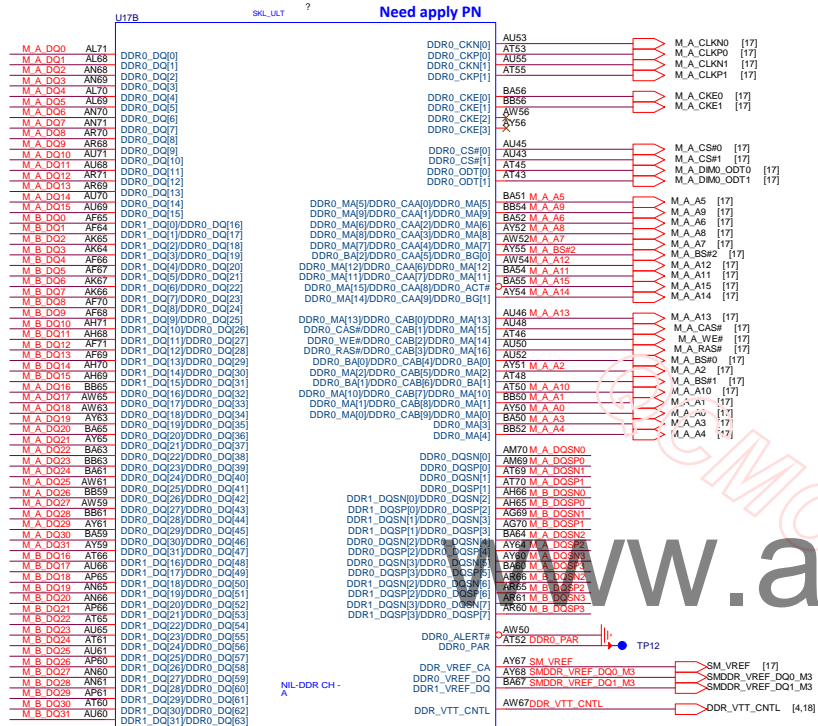
**PROJECT : X1A**  
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 - SKYPAKE 1/20(eDP/DDI)	1A
Date: Friday, May 22, 2015	Sheet	2 of 49

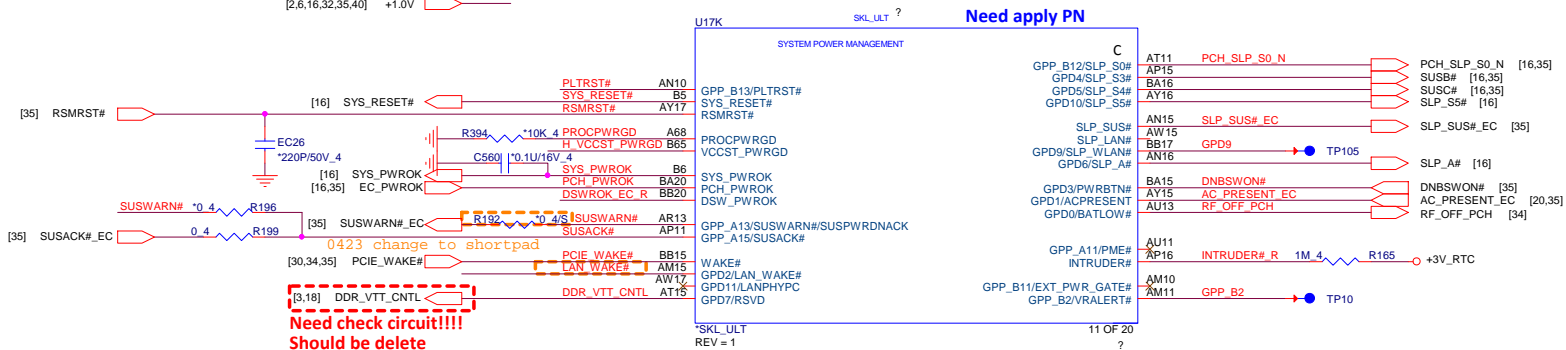
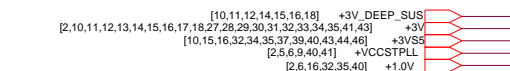
# SkyLake ULT Processor (DDR3L)

[17] M.A.DQSN7-0  
[17] M.A.DQSP7-0  
[18] M.B.DQSN7-0  
[18] M.B.DQSP7-0  
[17] M.A.DQ63-0  
[18] M.B.DQ63-0

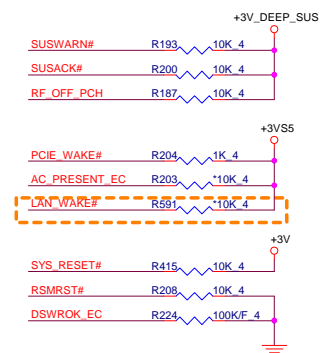
+1.35VSUS [6,17,18,38,40]



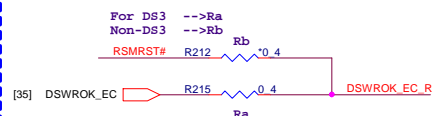
www.aitech.ru



## PCH Pull-high/low(CLG)

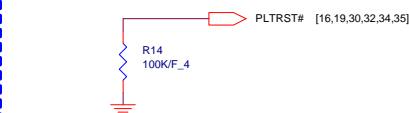


## For DS3 Sequence

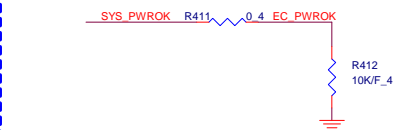


## PLTRST#(CLG)

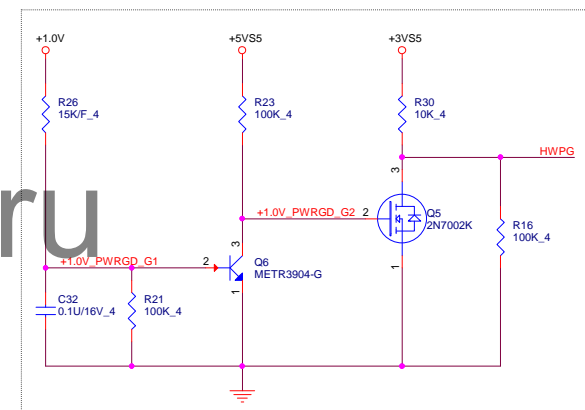
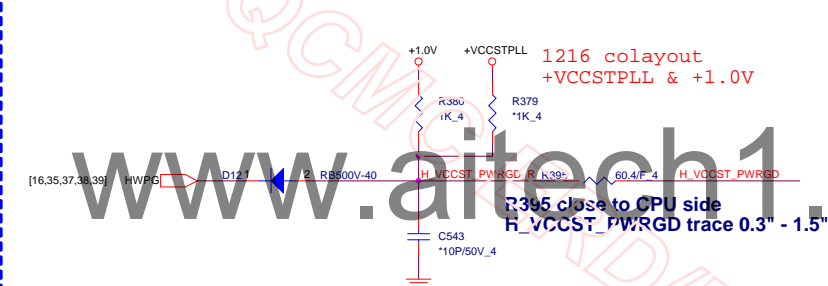
Check Q2010 Rise/Fall time less than 100ns



## System PWR\_OK(CLG)

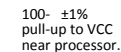


## For HWPG, +1.0V and +VCCSTPLL Sequence



1110 Add Citcuit for +1.0V Power Good




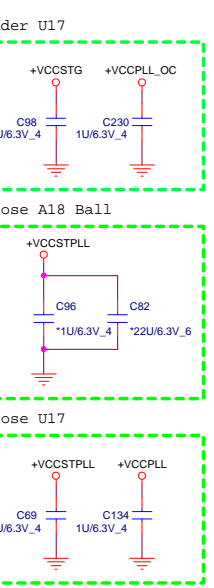


**CLOSE TO CPU  
PLACE THE PU RESISTORS**

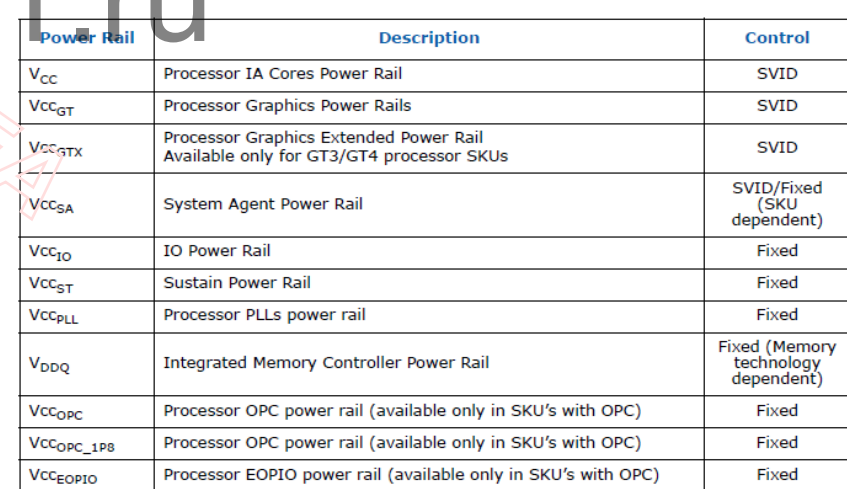
PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE

**CLOSE TO CPU  
PLACE THE PU RESISTORS**

	<b>PROJECT : X1A</b> Quanta Computer Inc.		
	Size Custom	Document Number 07 -- SKYPAKE 6/20 (POWER-1)	Rev 1A
	Date: Wednesday, May 13, 2015	Sheet	5 of 49

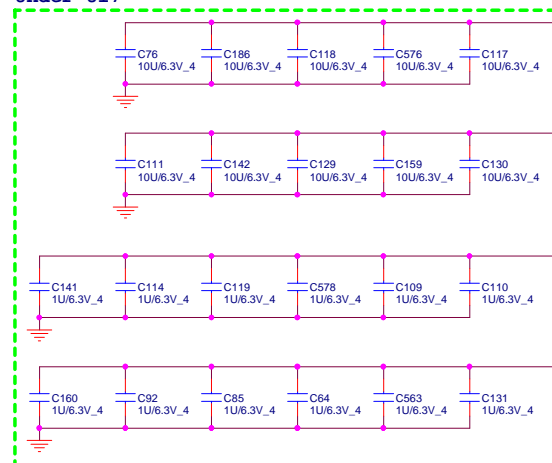


## 1226 Add thermistor circuit for CPU & DDR



+VCCGT [41]

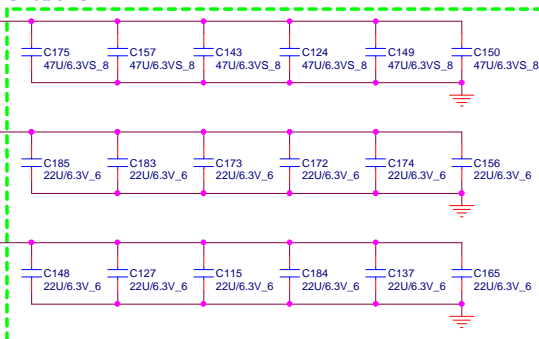
Under U17



Need apply PN

31A

Close U17

[41] VCCGT\_SENSE  
[41] VSSGT\_SENSEJ70  
J69SKL\_ULT  
REV = 1

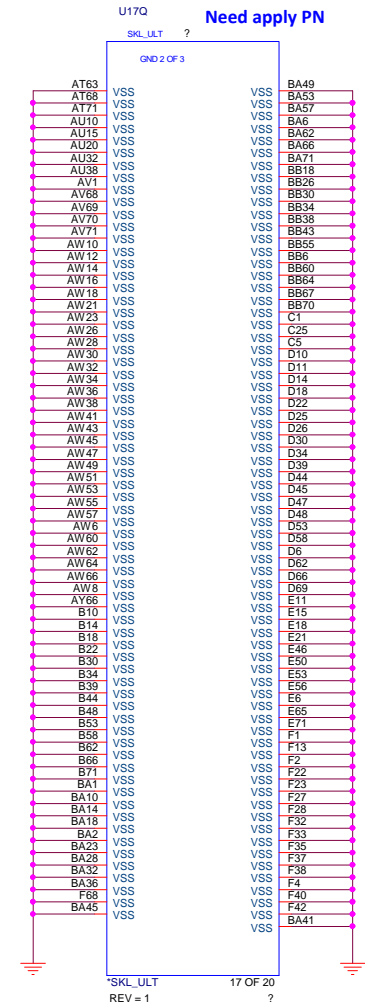
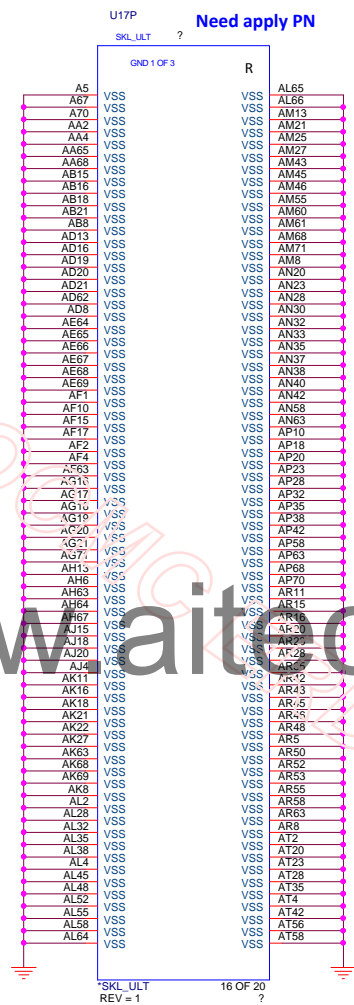
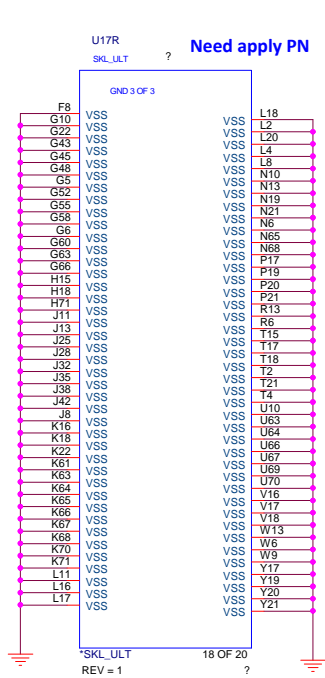
13 OF 20

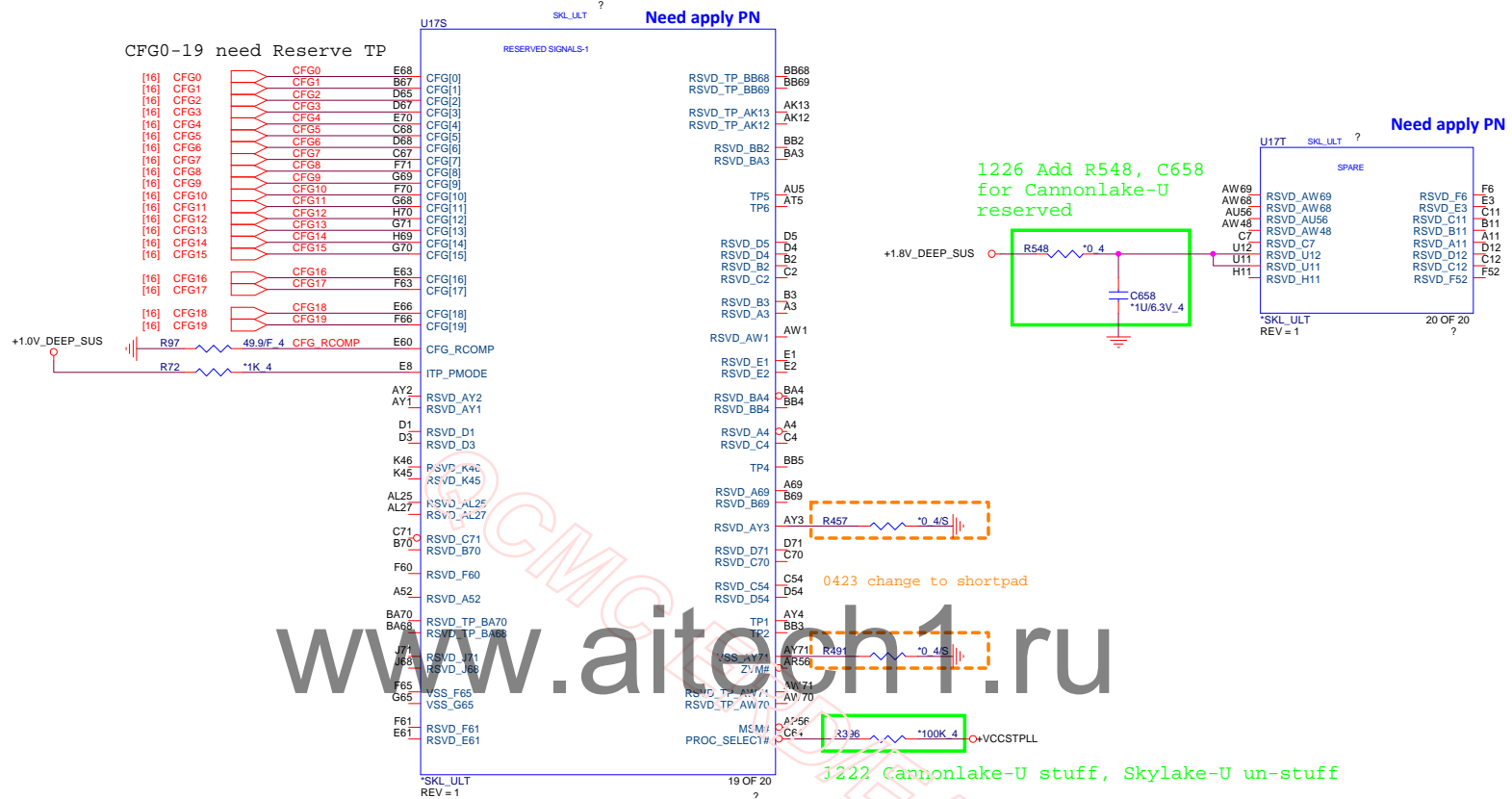
Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



**PROJECT : X1A**  
Quanta Computer Inc.

Size Custom	Document Number <b>09 – SKYPAKE 8/20 (POWER-3)</b>	Rev 1A
Date: Wednesday, May 13, 2015	Sheet	7 of 49

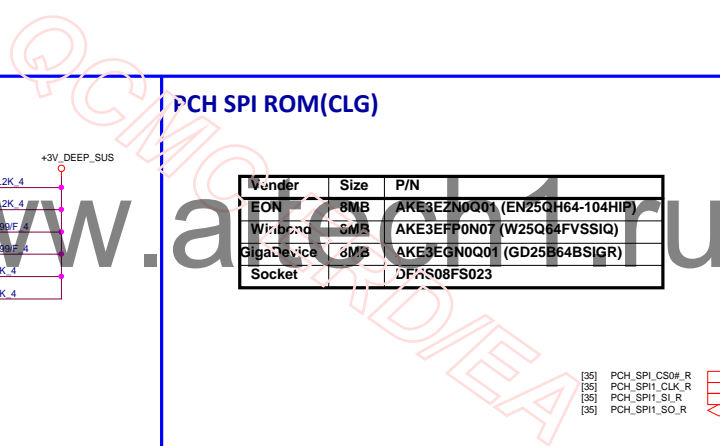




### Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

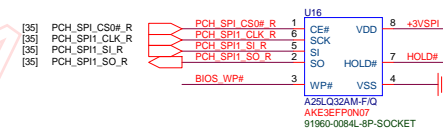
	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R387 *1K 4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R427 *1K 4



Timing diagram for the SPI interface. The signals and their connections are as follows:

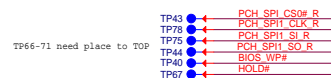
Signal	Pin	Value
SMB_PCH_CLK	R91	2.2K
SMB_PCH_DAT	R88	2.2K
SMB_ME0_CLK	R103	499F
SMB_ME0_DAT	R442	499F
SMB_ME1_CLK	R439	1K
SMB_ME1_DAT	R436	1K

The signals are connected to a +3V DEEP\_SUS supply.

4M SPI ROM Socket

U15&U16 footprint 要重疊

CPU heat pipe local thermal sensor  
DDR thermal sensor  
RTD2136  
EC

[illegible]

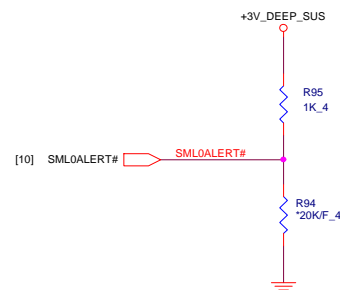
1222 change R409,R437 from 3.3K 1% to 1K 5%

# Functional Strap Definitions

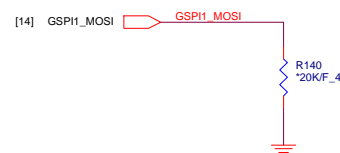
**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET



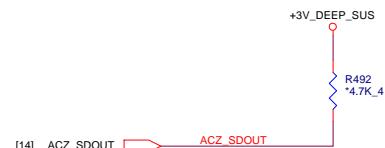
**TOP SWAP OVERRIDE**  
HIGH - TOP SWAP ENABLE  
LOW-DISABLED  
HIGH: LPC SELECTED FOR SYSTEM FLASH  
WEAK INTERNAL PD



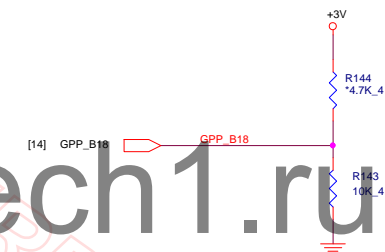
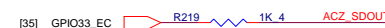
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).  
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



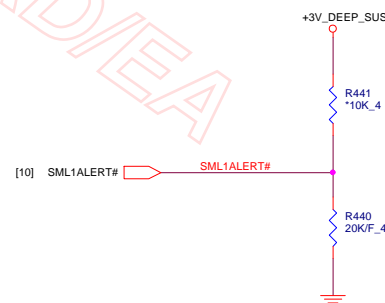
**No Boot:**  
The signal has a weak internal pull-down.  
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.  
Bit 10      Boot BIOS Destination  
0            SPI  
1            LPC



**No Boot:**  
The signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.

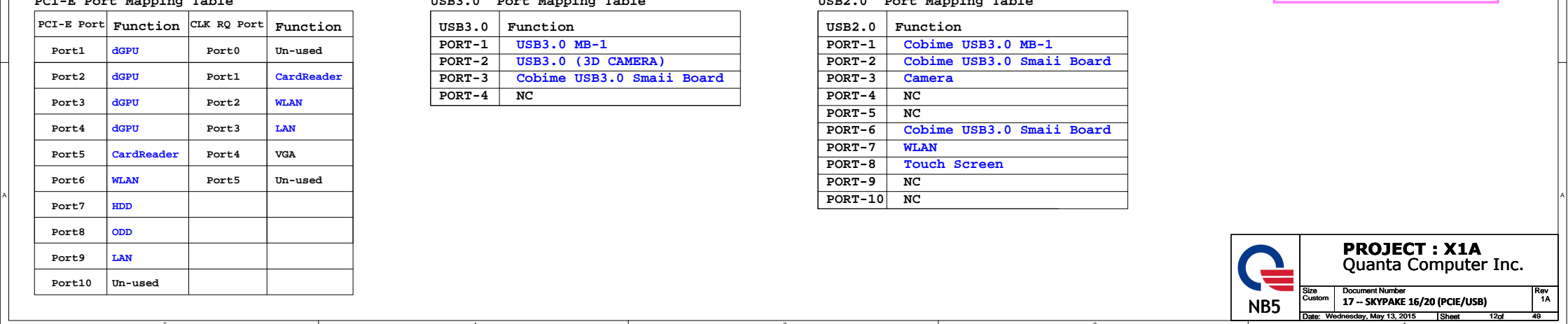


**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable No Reboot mode.  
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature).  
This function is useful when running ITP/XDP.

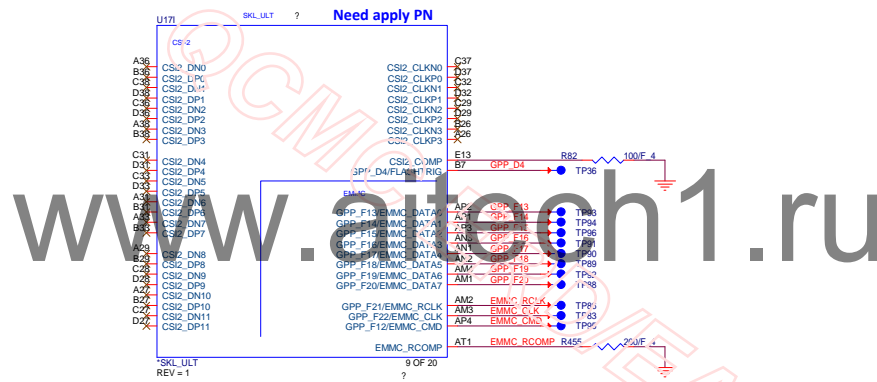
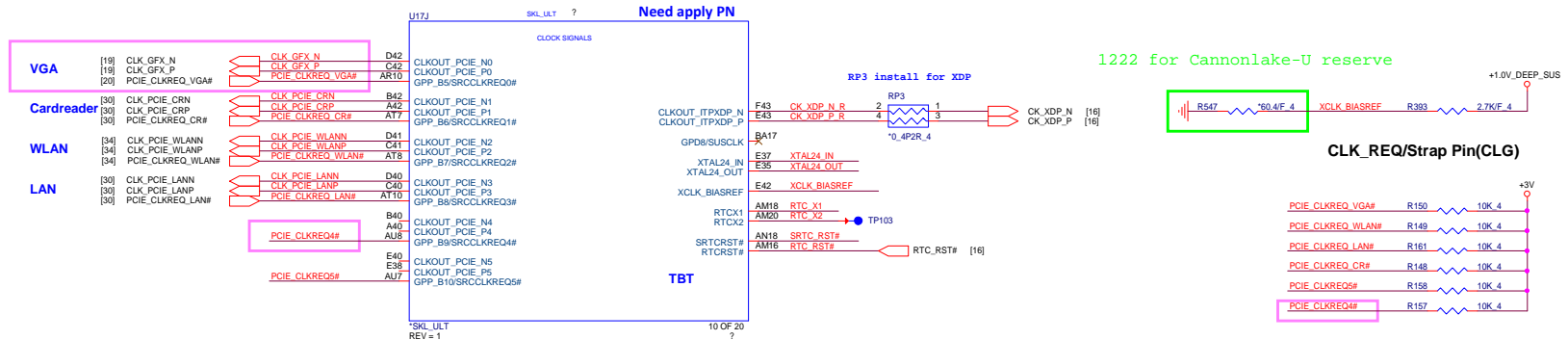


**No Boot:**  
The signal has a weak internal pull-down.  
0 = LPC Is selected for EC.  
1 = eSPI Is selected for EC.

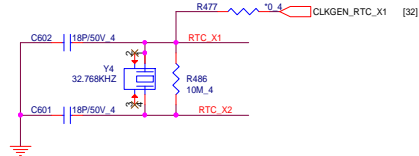




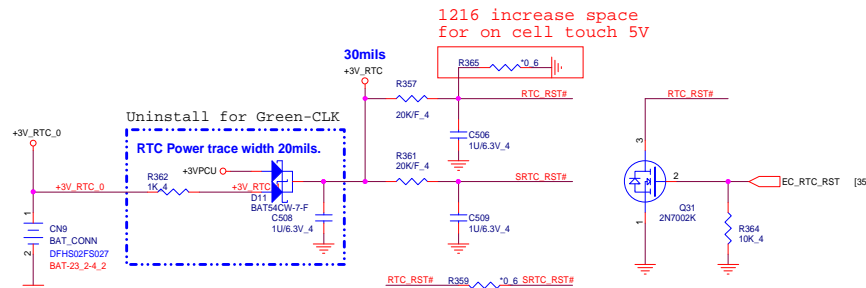
+3V\_RTC [4,15,32]  
 +1.8V\_DEEP\_SUS [9,15,30,46]  
 +3V [2,4,10,11,12,14,15,16,17,18,27,28,30,31,32,33,34,35,41,43]



## RTC Clock 32.768KHz



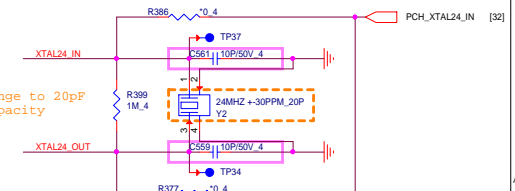
## RTC Circuitry(RTC)



## External Crystal and Green Clock

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

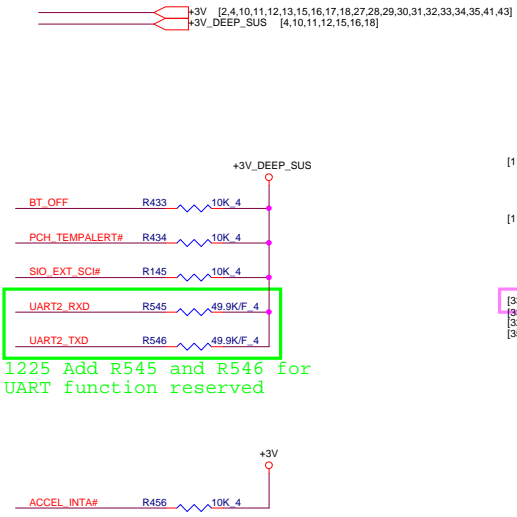
0513 Y2 change to 20pF internal capacity



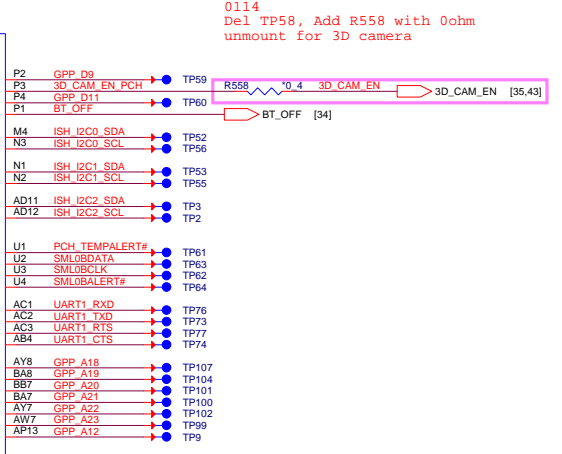
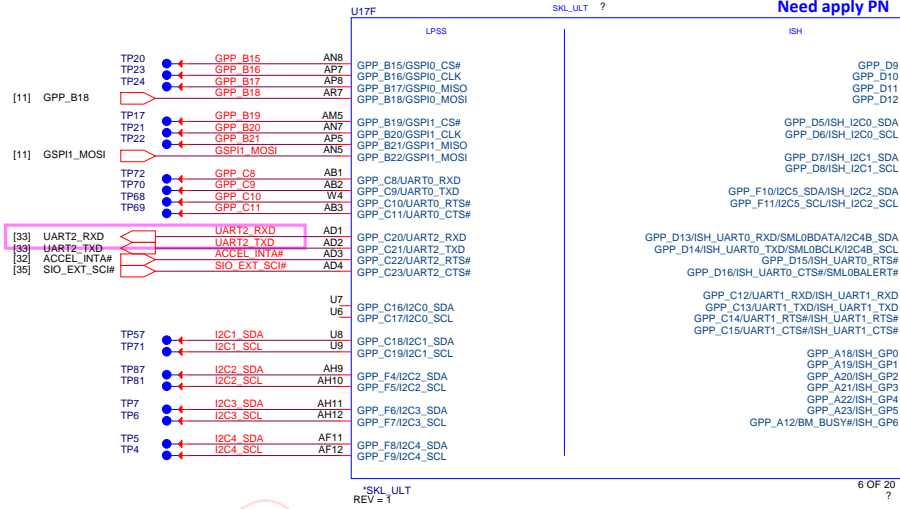
**PROJECT : X1A**  
Quanta Computer Inc.

Size Custom  
 Document Number  
 13 - SKYPAKE 17/20 (CLK)  
 Date: Wednesday, May 13, 2015  
 Sheet 13 of 48  
 Rev 1A

Skylake (GPIO)

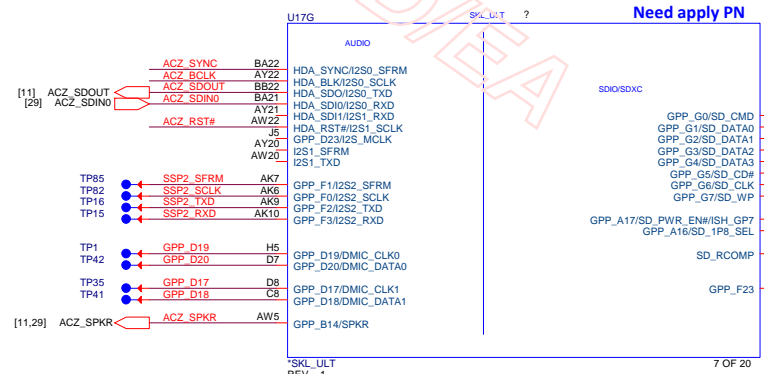
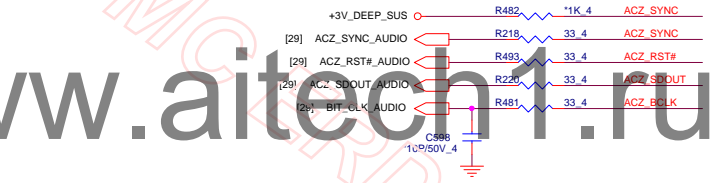
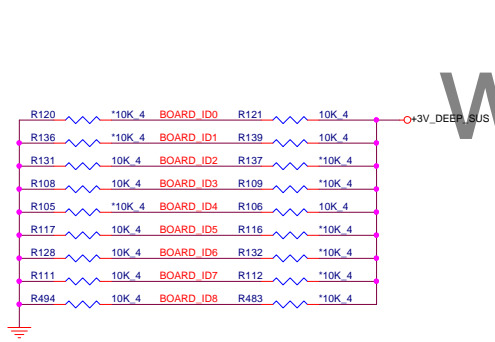


1225 Add R545 and R546 for UART function reserved




0114 Del TP58, Add R558 with 0ohm unmount for 3D camera  
R558 0 4 3D\_CAM\_EN [35,43]  
BT\_OFF [34]

HDA Bus(CLG)



0129 Del TP108 add GPP\_A16  
GPP\_A16 [33]  
R123 200/F 4  
AF13 GPP\_F23 TP84

Skylake U	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID[0]
Model	ID8 ID7	ID6 ID5	ID4 ID3	ID2 ID1	ID0
Definition	00 : non 3D SKU 01 : 3D SKU	00 : Crunch1.0 01 : Crunch2.0	00 : I+N Single(X1B-6L) 01 : I+N Dual(X1B-10L) 10 : I+A Single(X1A-6L) 11 : Reserve	00 : 14" 01 : 15" 10 : 17" 11 : Reserve	0 : UMA 1 : DIS



PROJECT : X1A  
Quanta Computer Inc.

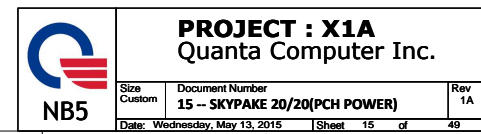
Size Custom

Document Number 20 - SKYPAKE 19/20 (GPIO)

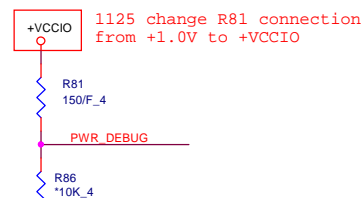
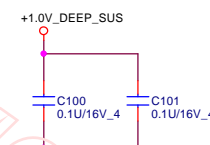
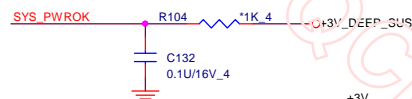
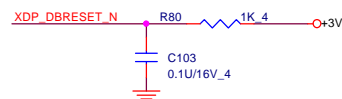
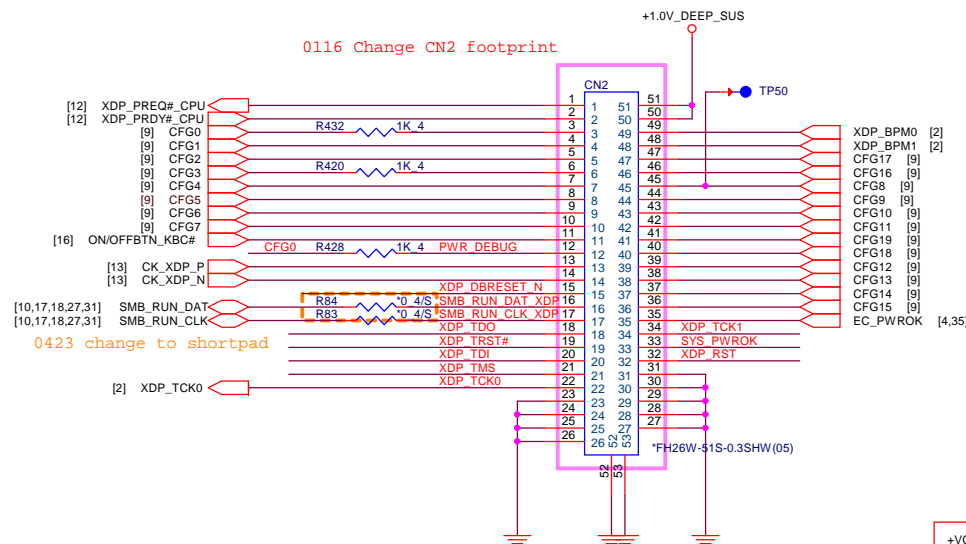
Date: Wednesday, May 13, 2015

Rev 1A

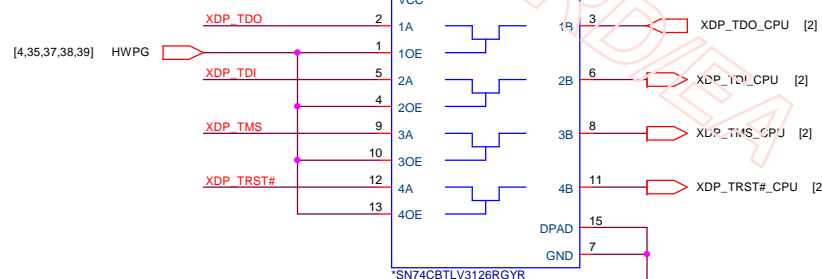
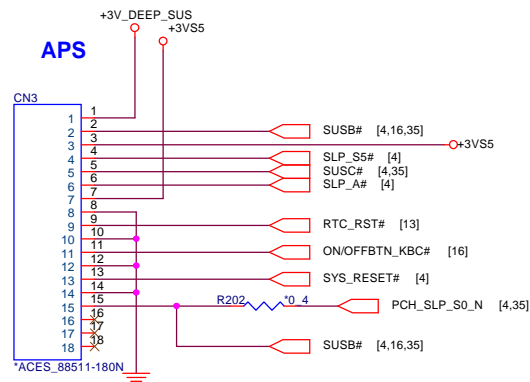
14 of 49



0116 Change CN2 footprint



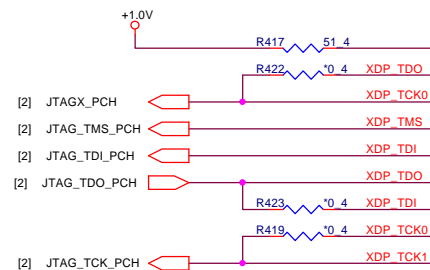
APS



[4] SYS\_PWROK

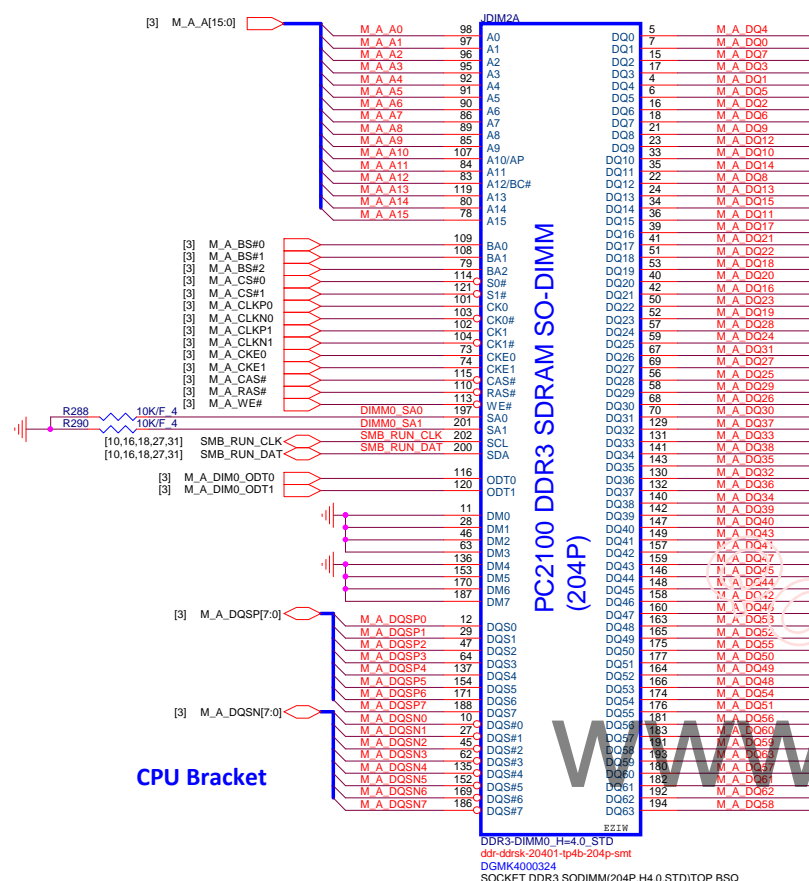
[4,19,30,32,34,35] PLTRST#

[2,6,40] +VCCIO



**PROJECT : X1A**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>16 -- HSW XDP &amp; APS</b>	<b>1A</b>
Date: Wednesday, May 13, 2015	Sheet 16 of 49	



M\_A\_DQ[63:0] [3]

PV modify to short pad

[18] PM\_EXTTS#0

[3,18] DDR3\_DRAMRST#

SMDDR\_VREF\_DQ0\_M1

R286

0.6/5

+SMDDR\_VREF\_DIMM

+SMDDR\_VREF\_DIMM

+SMDDR\_VREF\_DIMM

+SMDDR\_VREF\_DIMM

+SMDDR\_VREF\_DIMM

+SMDDR\_VREF\_DIMM

+SMDDR\_VREF\_DIMM

+SMDDR\_VREF\_DIMM

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+SMDDR\_VREF\_DIMM

+SMDDR\_VREF\_DIMM

+SMDDR\_VREF\_DIMM

+SMDDR\_VREF\_DIMM

+SMDDR\_VREF\_DIMM

+SMDDR\_VREF\_DIMM

2.48A

+1.35VSUS

IDIM2B

VDD1 75  
VDD2 76  
VDD3 81  
VDD4 82  
VDD5 87  
VDD6 88  
VDD7 93  
VDD8 94  
VDD9 99  
VDD10 100  
VDD11 105  
VDD12 106  
VDD13 111  
VDD14 112  
VDD15 117  
VDD16 118  
VDD17 123  
VDD18 124VSS16 44  
VSS17 48  
VSS18 49  
VSS19 54  
VSS20 55  
VSS21 61  
VSS22 66  
VSS23 67  
VSS24 71  
VSS25 72  
VSS26 78  
VSS27 83  
VSS28 84  
VSS29 89  
VSS30 90  
VSS31 95  
VSS32 96  
VSS33 101  
VSS34 102  
VSS35 107  
VSS36 108  
VSS37 113  
VSS38 114  
VSS39 119  
VSS40 120  
VSS41 125  
VSS42 126  
VSS43 131  
VSS44 132  
VSS45 137  
VSS46 138  
VSS47 143  
VSS48 144  
VSS49 149  
VSS50 150  
VSS51 155  
VSS52 156VSS1 2  
VSS2 3  
VSS3 8  
VSS4 9  
VSS5 13  
VSS6 14  
VSS7 19  
VSS8 20  
VSS9 25  
VSS10 26  
VSS11 31  
VSS12 32  
VSS13 37  
VSS14 38  
VSS15 43VTT1 203  
VTT2 204  
GND 205  
GND 206

+0.65V\_DDR\_VTT

+3V

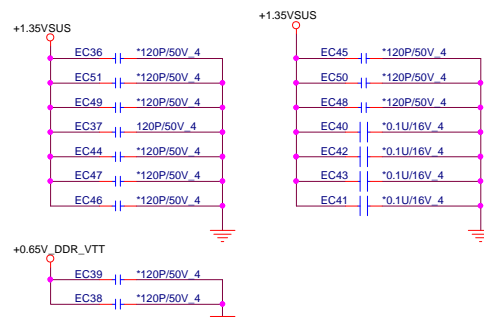
R311 10K/F 4

NC1 77  
NC2 122  
NCTEST 125  
EVENT# 198  
RESET# 30VREF\_DQ 1  
VREF\_CA 126

PC2100 DDR3 SDRAM SO-DIMM (204P)

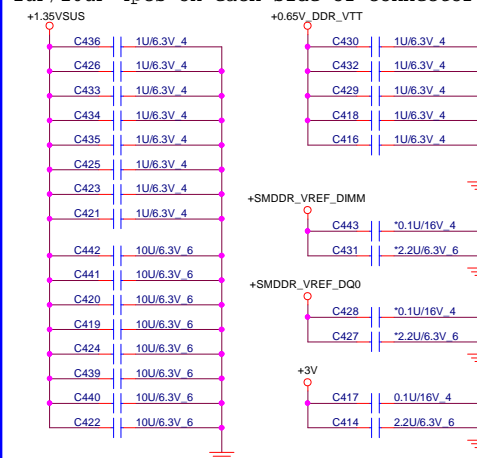
DDR3-DIMM0\_H=4.0 STD  
ddr-ddrsk-20401-tp4b-204p-smt  
SOCKET DDR3 SODIMM(204P,H4.0,STD)TOP BSQ[2,4,10,11,12,13,14,15,16,18,27,28,29,30,31,32,33,34,35,41,43]  
[3,6,18,38,40] +1.35VSUS  
[18,38] +0.65V\_DDR\_VTT  
[18] +SMDDR\_VREF\_DIMM

## For EMI RESERVE

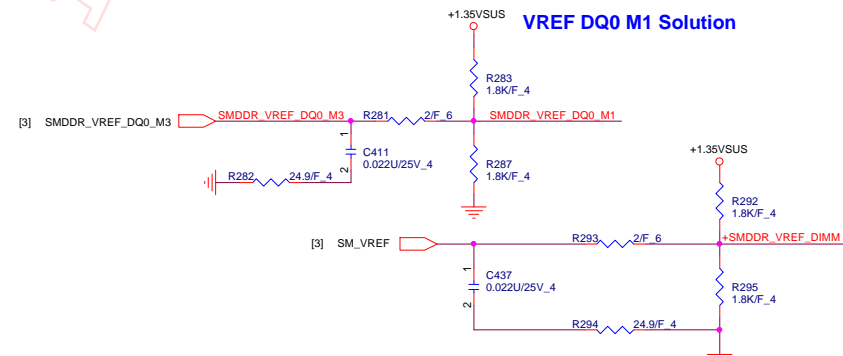


## Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector

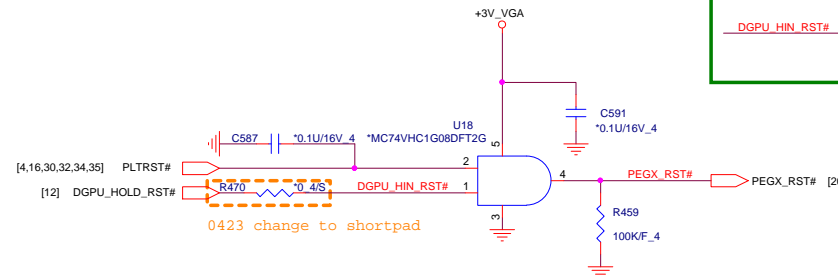
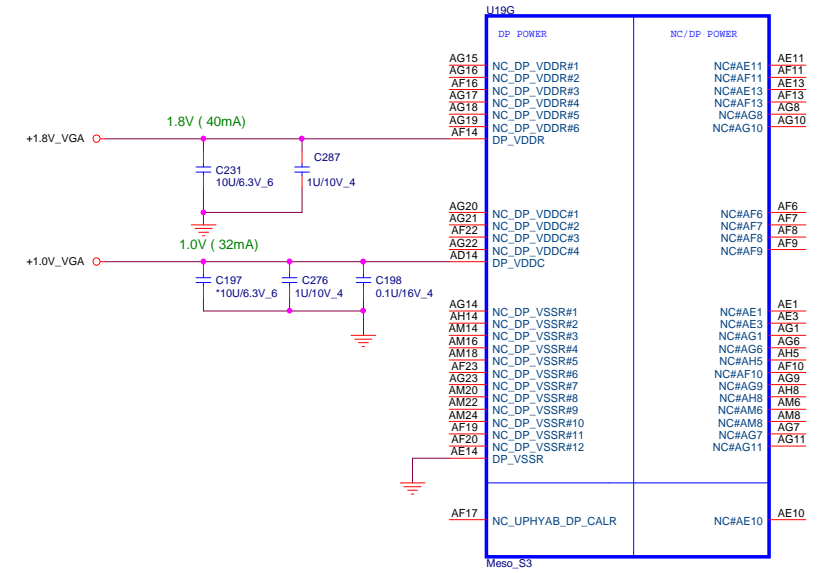


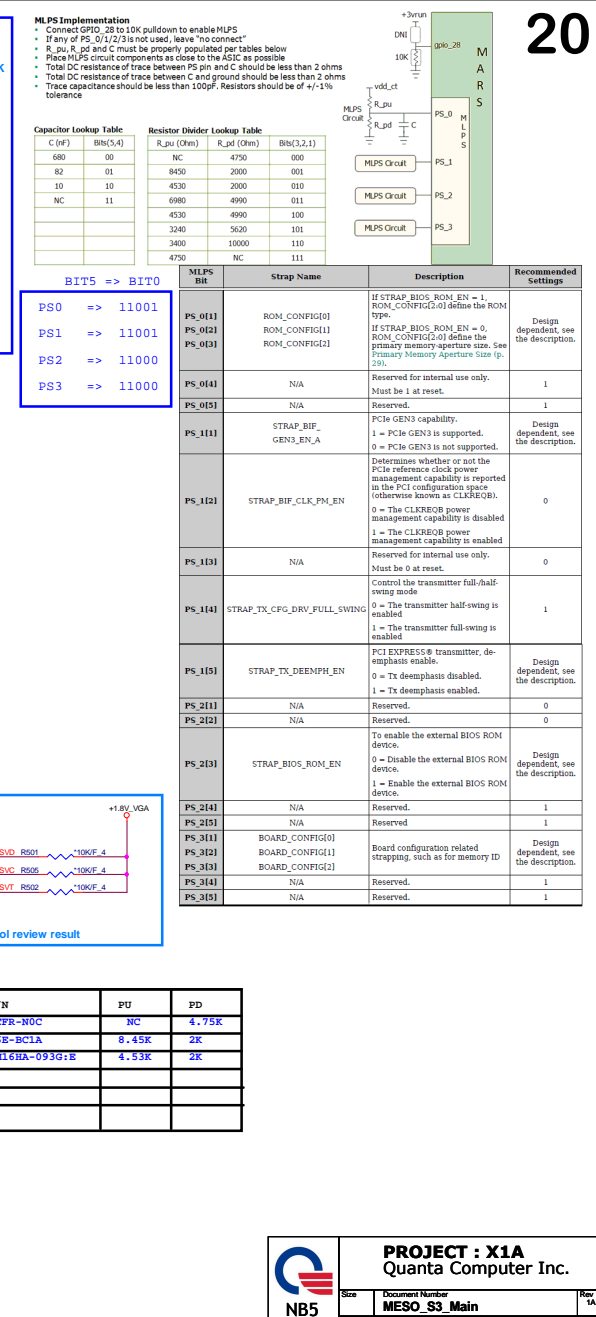
## VREF DQ0 M1 Solution

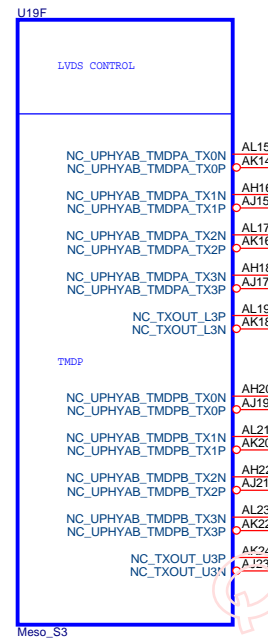
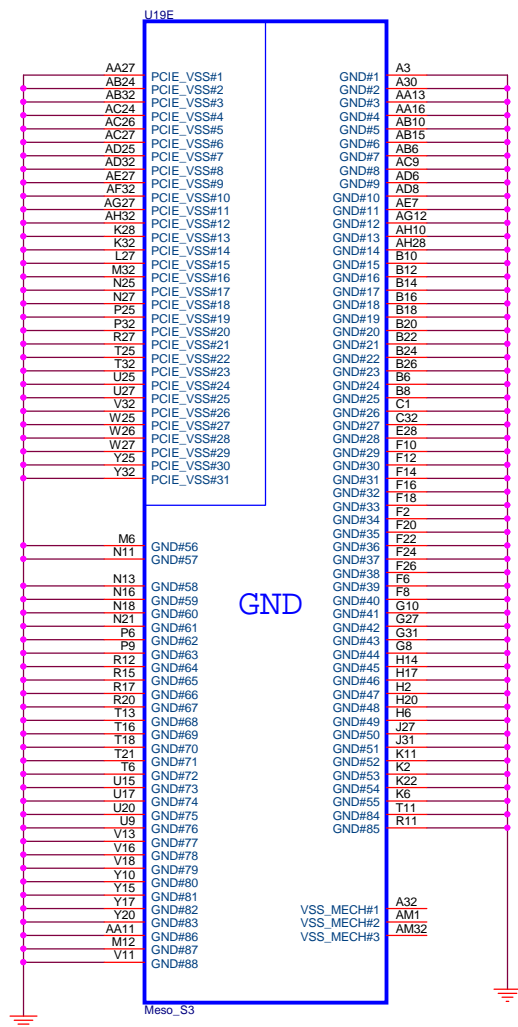












### CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1= INSTALL 3K RESISTOR  
X= DESIGN DEPENDANT  
NA= NOT APPLICABLE

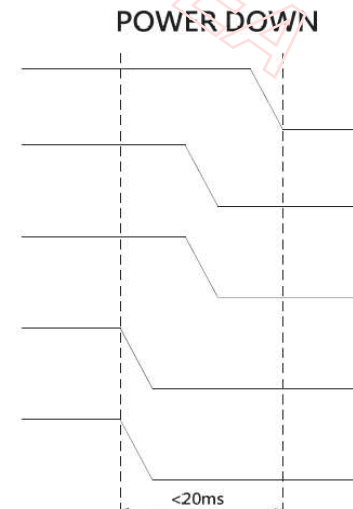
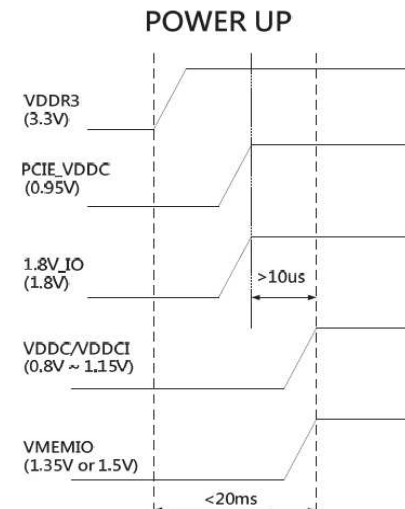
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/W/histler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

### NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

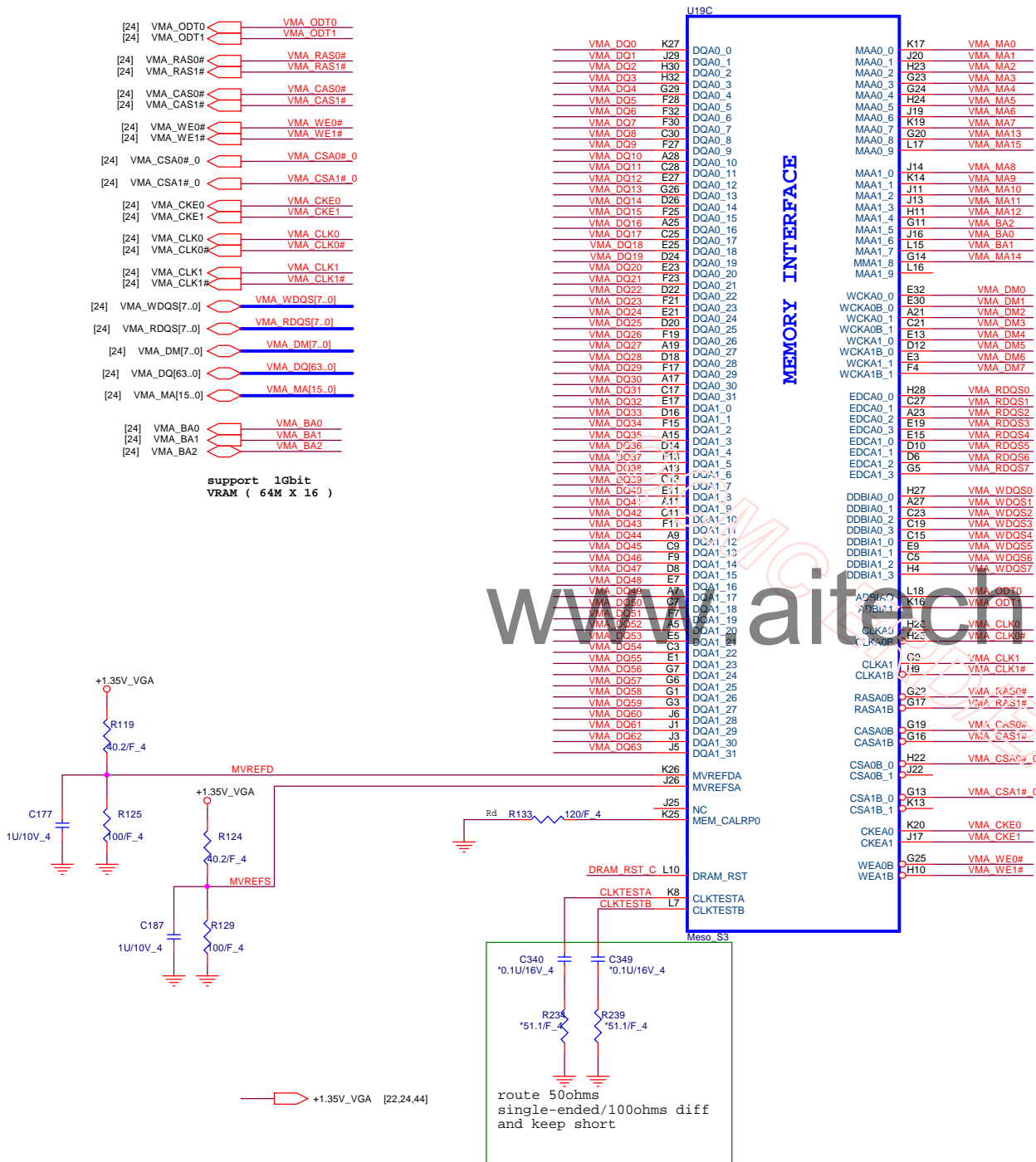
### POWER UP / POWER DOWN SEQUENCE

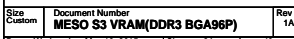


**PROJECT : X1A**  
Quanta Computer Inc.


Size	Document Number	Rev
	<b>MESO_S3_GND/LVDS/Strap</b>	1A
Date:	Wednesday, May 13, 2015	Sheet 21 of 49








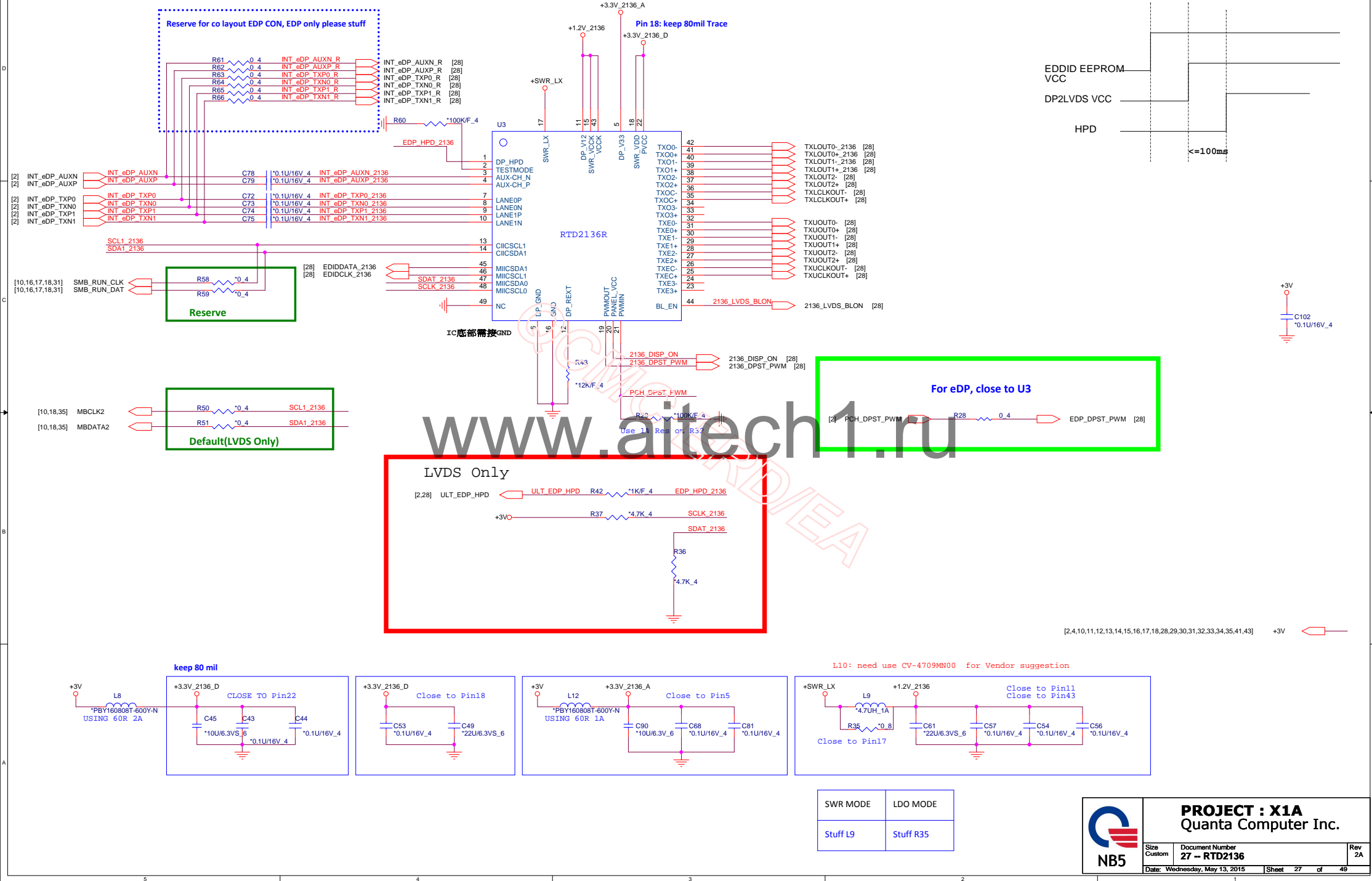
www.aitech1.ru

 NB5	<b>PROJECT : X1A</b> Quanta Computer Inc.		
	Size Custom	Document Number DDR3L - RANK1	Rev 1A
	Date: Wednesday, May 13, 2015		Sheet 25 of 49

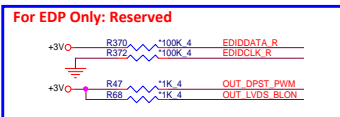
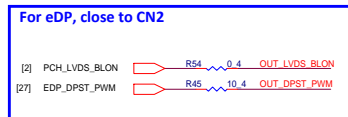
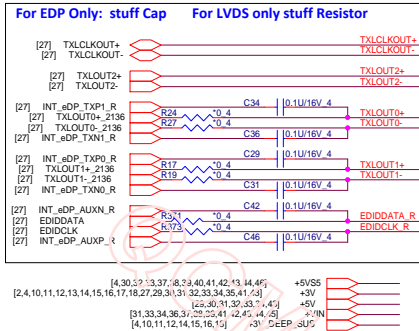
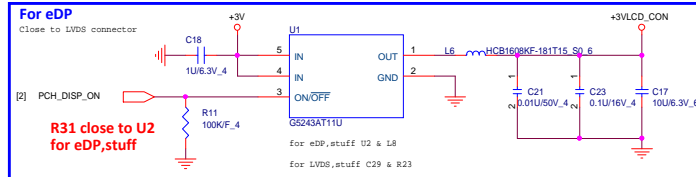
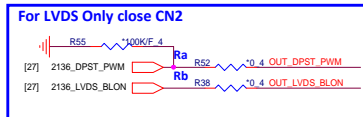
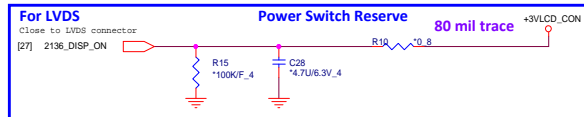
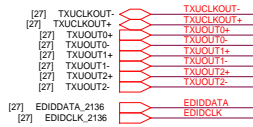
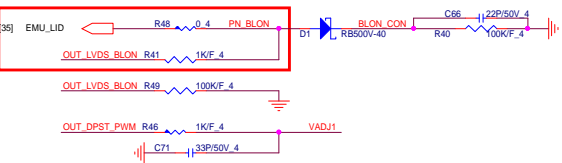
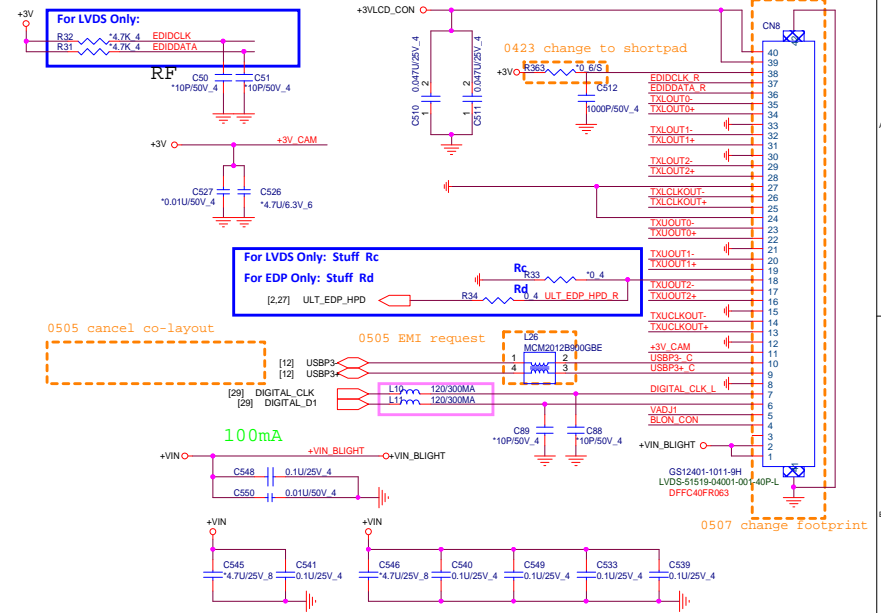


www.aitech1.ru

 NB5	<b>PROJECT : X1A</b> Quanta Computer Inc.			
	Size Custom	Document Number DDR3L - RANK1		Rev 1A
	Date: Wednesday, May 13, 2015		Sheet 26	of 49

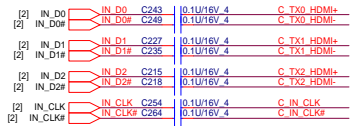


## LID Switch

**LVDS Conn.**

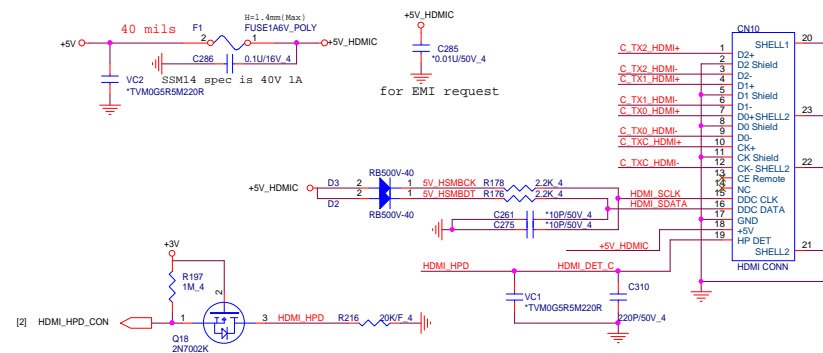
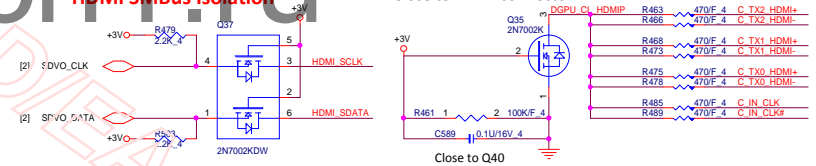
## 28

## HDMI Re-driver

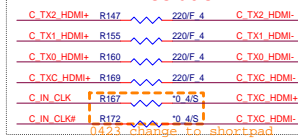


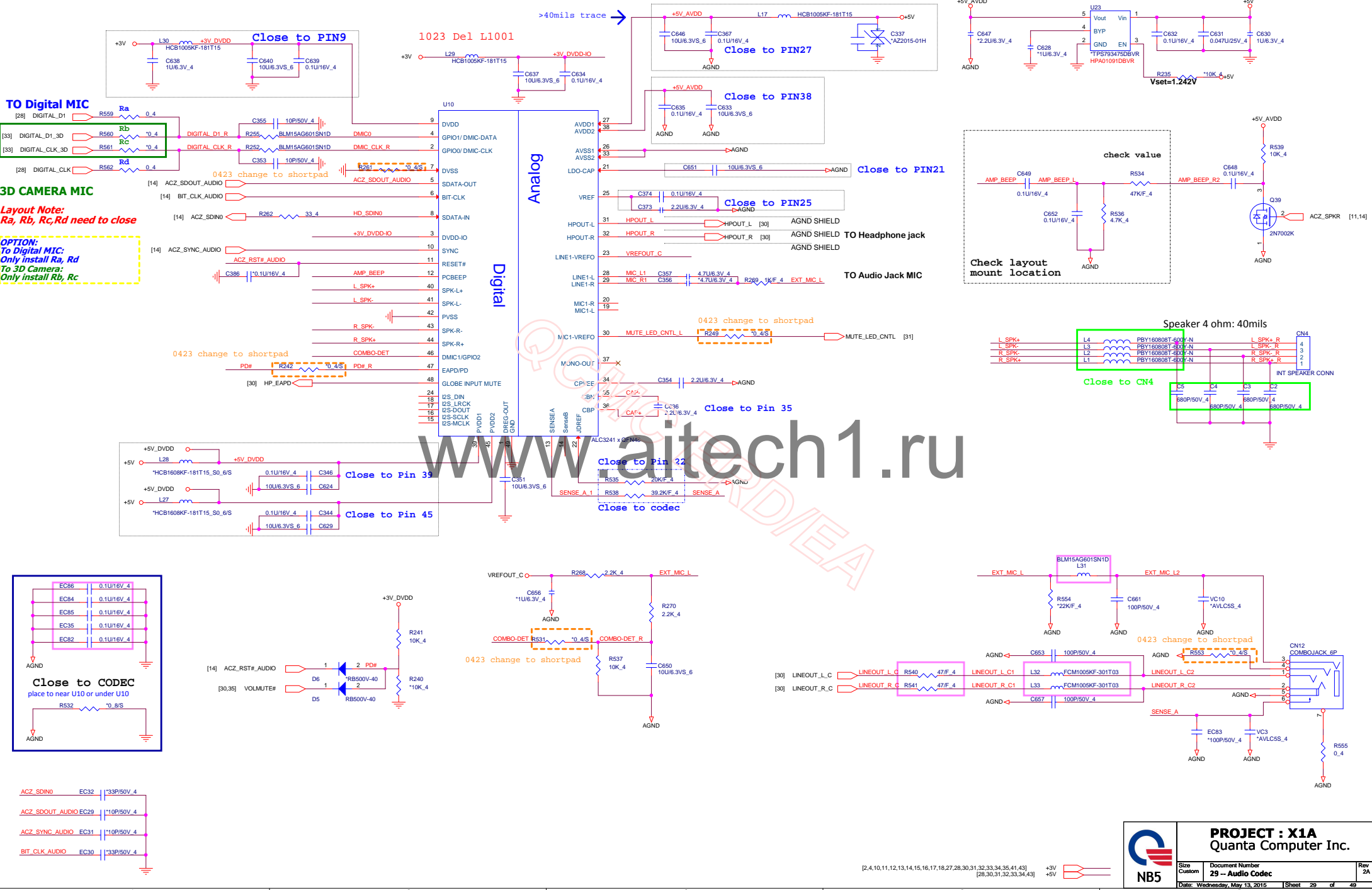
## HDMI CONN

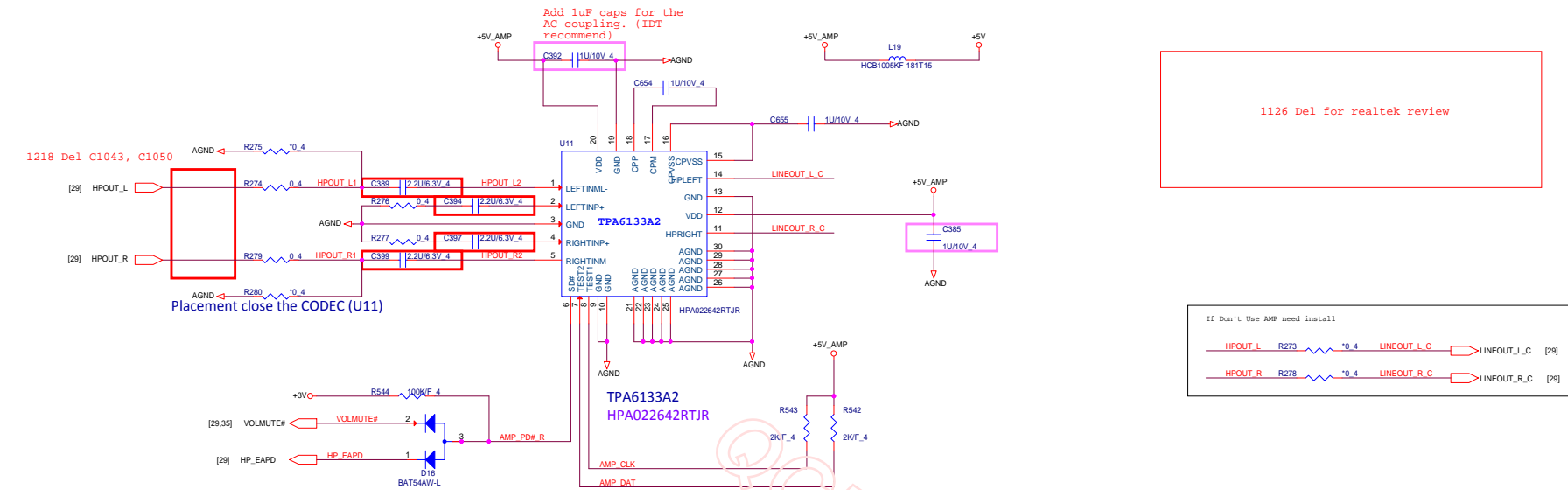
## HDMI SMBus Isolation



## EMI Solution







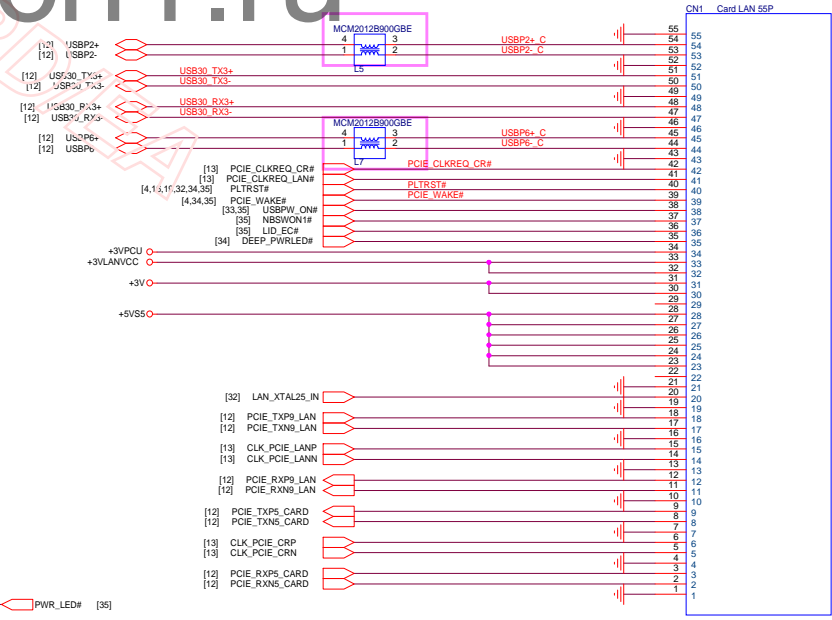
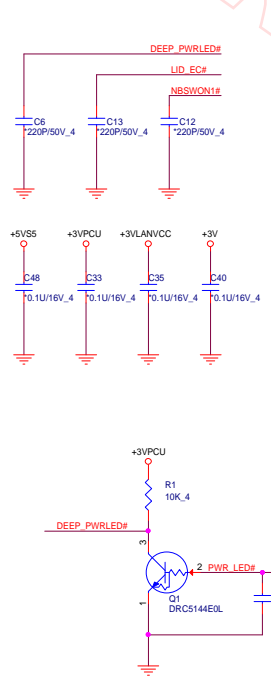
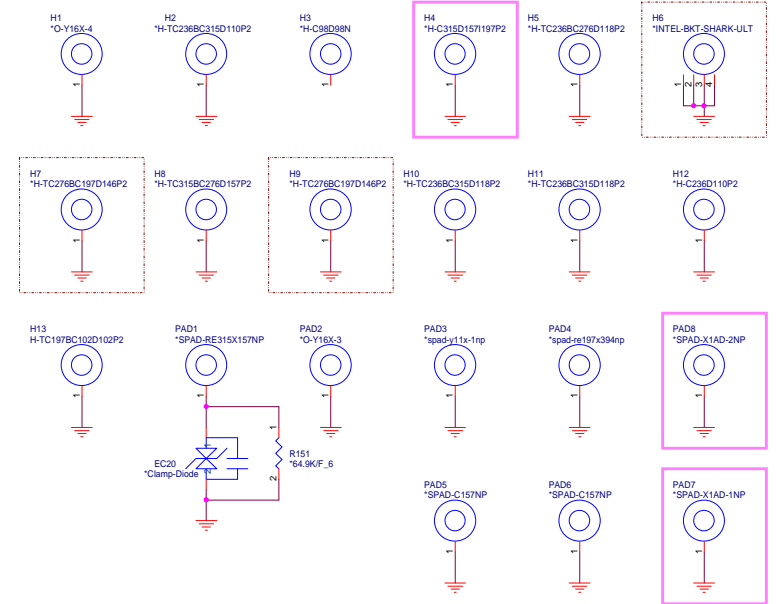
If Don't Use AMP need install

HPOUT\_L R273 \*0.4 LINEOUT\_L\_C [29]

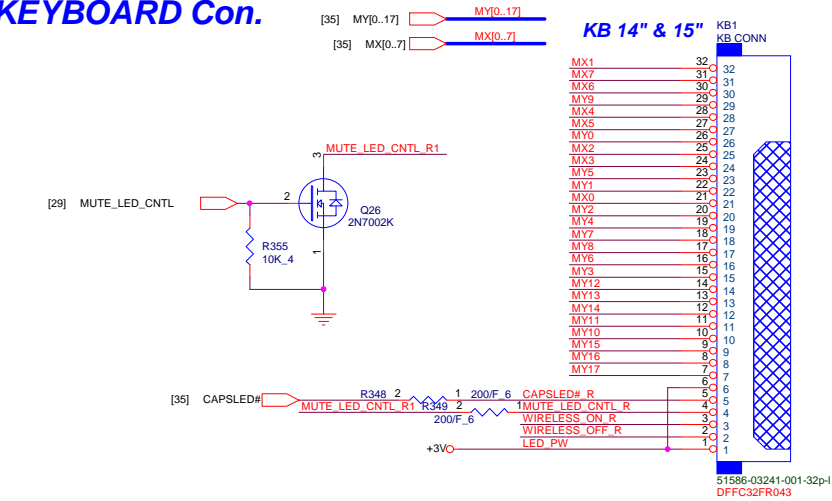
HPOUT\_R R278 \*0.4 LINEOUT\_R\_C [29]

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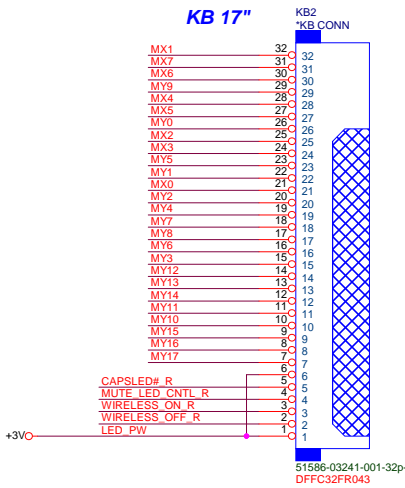
**HOLE**



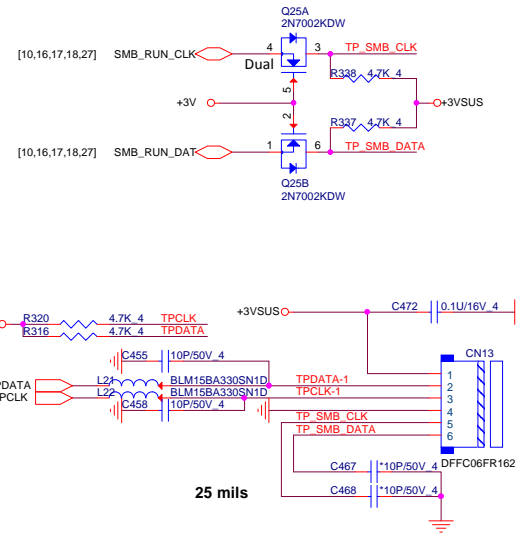
KEYBOARD Con.



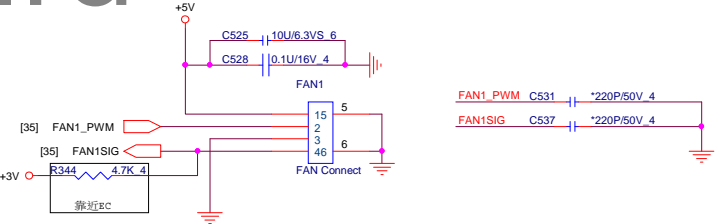
KB 17"



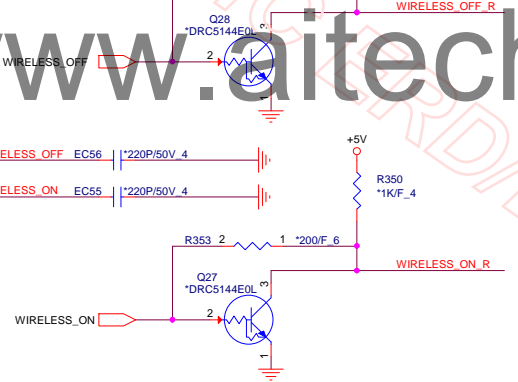
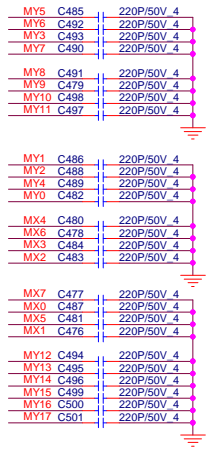
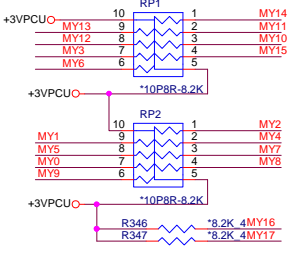
Touch Pad Connector



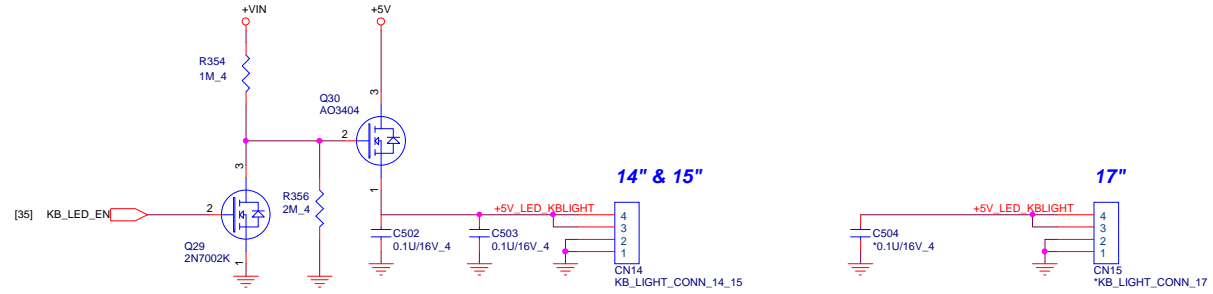
FAN CONN



KEYBOARD PULL-UP

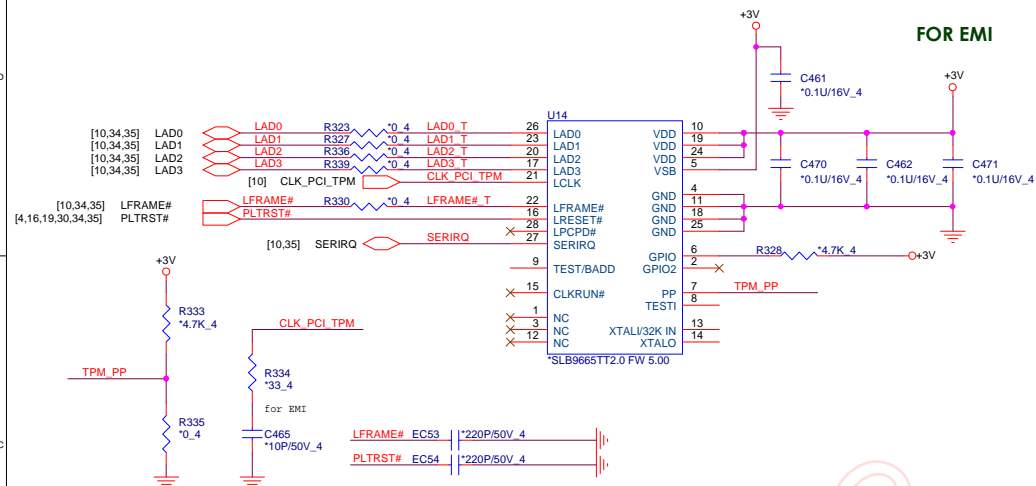


KB LIGHT CONN

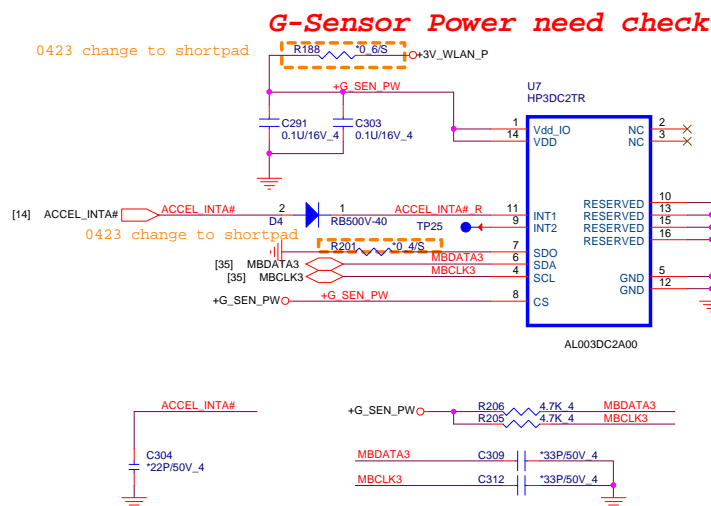


## TPM (2.0)

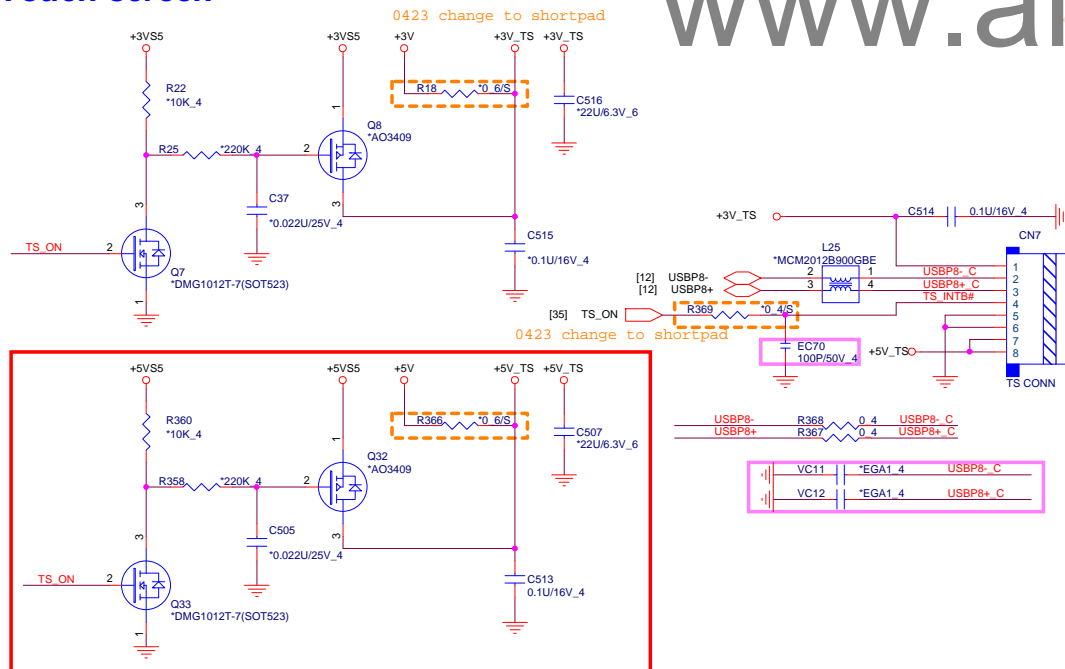
Address	
	BADD
HIGH	4EH/4F (default)



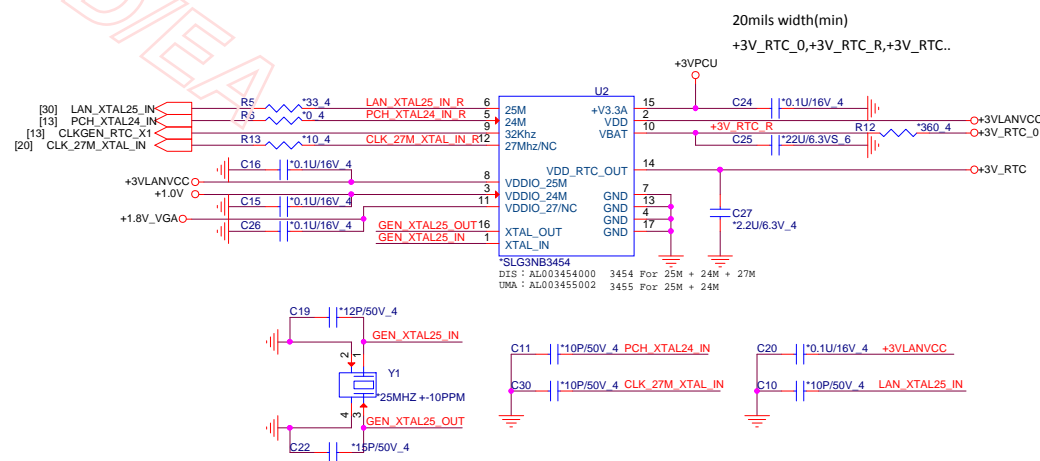
## Accelerometer Sensor



## Touch screen

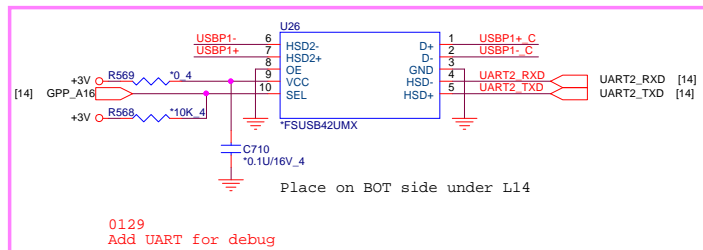


## Green CLK Circuitry

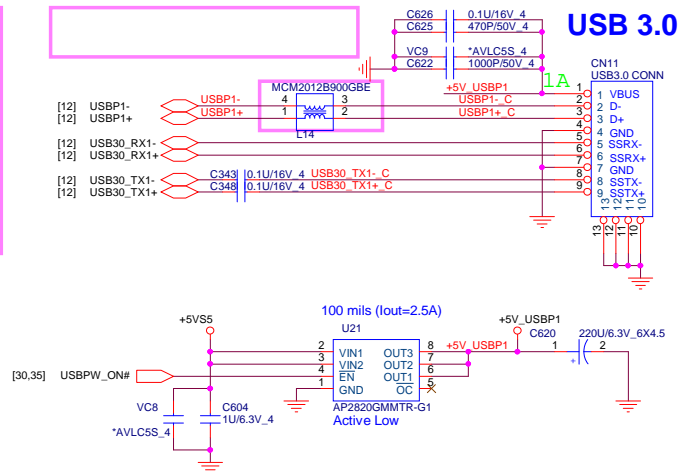




## UART for DEBUG



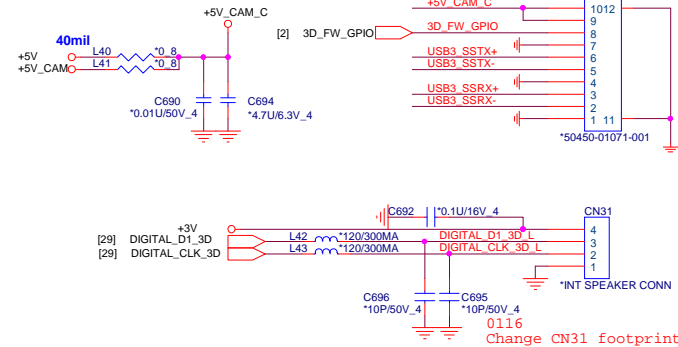
## USB 2.0/3.0 Combo



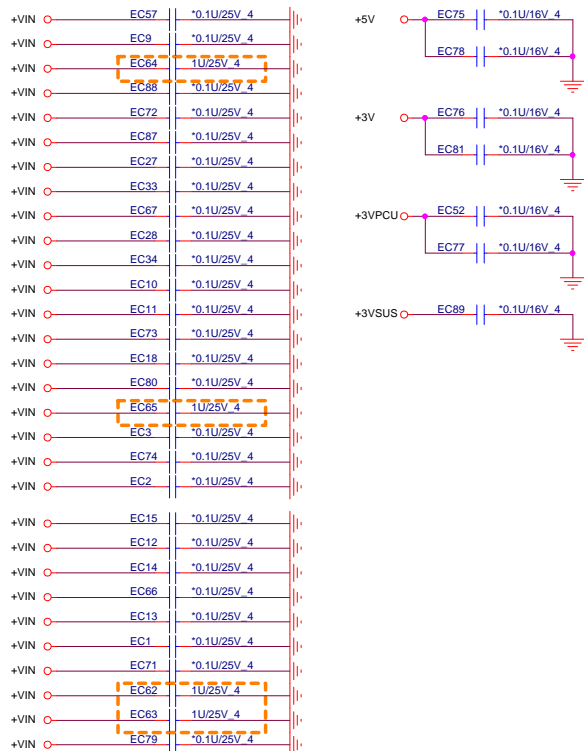
## USB 3.0

## 3D CAMERA

0114  
Add 3D CAMERA circuit



## EMI CAP



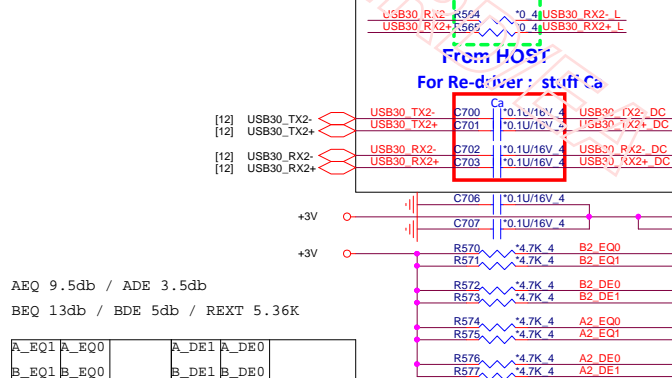
## USB3.0 re-driver for 3D CAMERA

Need close

non-USB 3.0 re-driver : stuff Ra

From HOS?

For Re-driver : stuff Ca

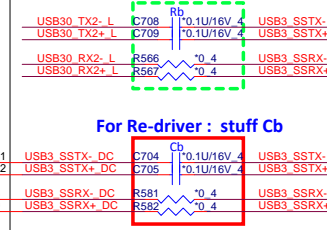


A_EQ1	A_EQ0	A_DE1	A_DE0				
0	0	0	0	9.5db	0	0	3.5db
0	1	13db	0	1	no de-emphasis		
1	0	4.5db	1	0	2.7db		
1	1	7.5db	1	1	5db		

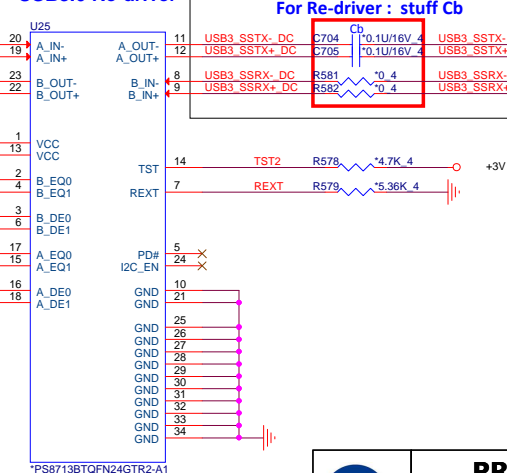
TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing

Need close

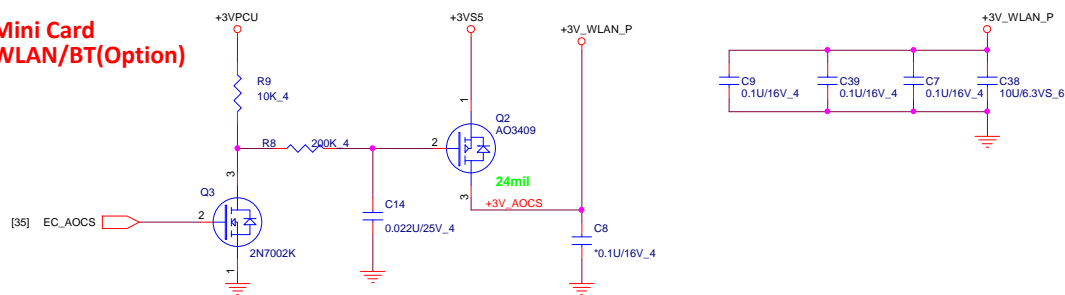
non-USB 3.0 re-driver : stuff Rb



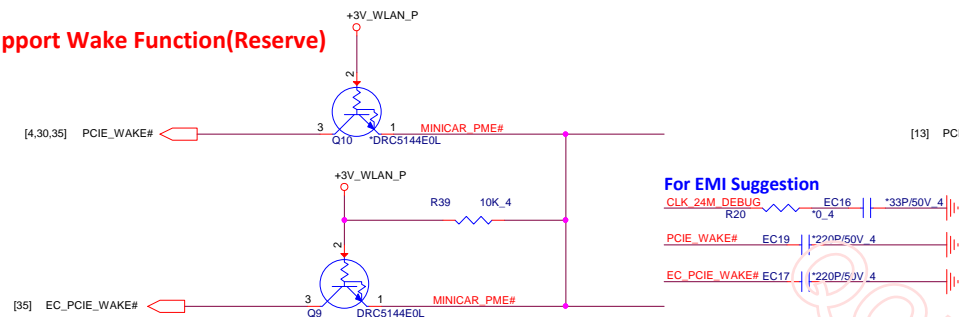
## USB3.0 Re-driver



**Mini Card  
WLAN/BT(Optional)**



## Support Wake Function(Reserve)

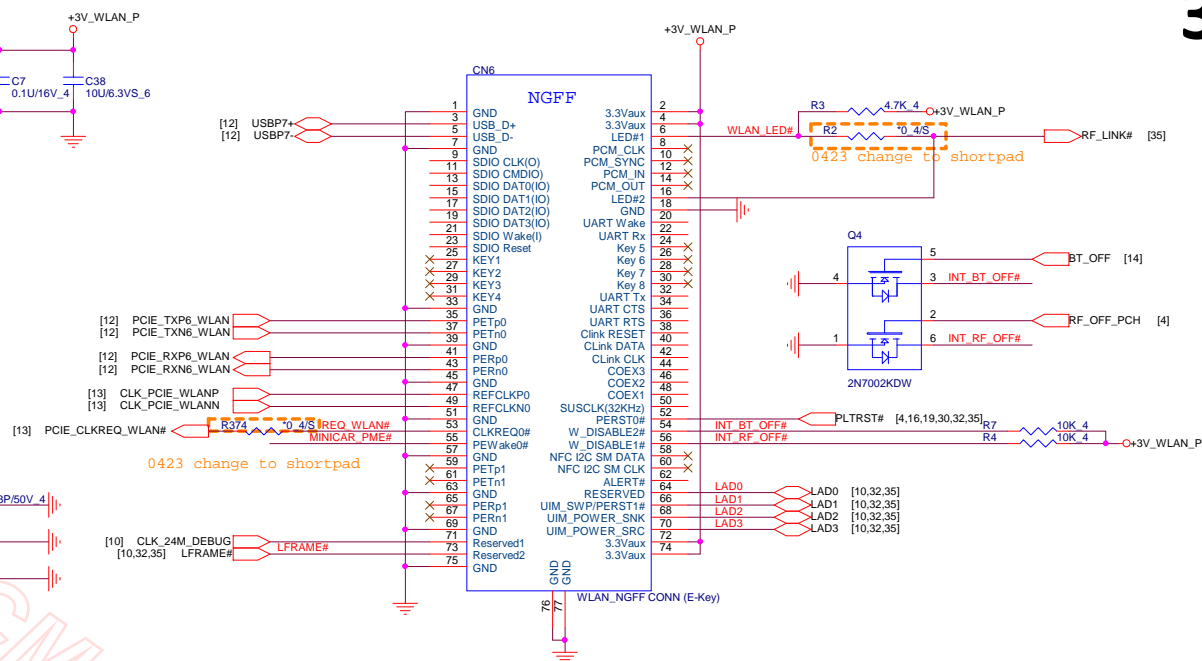


### For EMI Suggestion

CLK 24M DEBUG EC16 \*33P/50V 4  
R20 \*0\_4

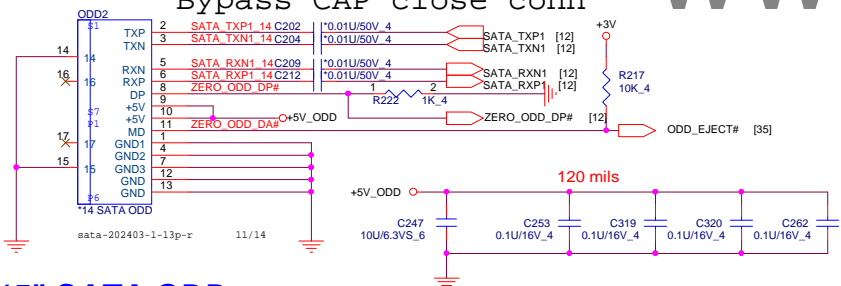
PCIE\_WAKE# EC19 \*220P/50V 4

EC\_PCIE\_WAKE# EC17 \*220P/5JV 4

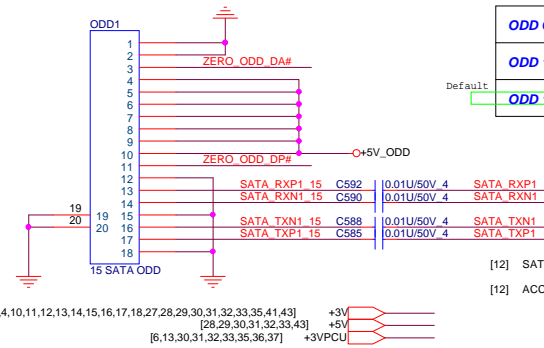


## 14" SATA ODD

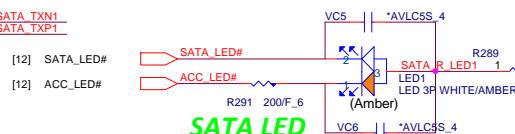
Bypass CAP close conn



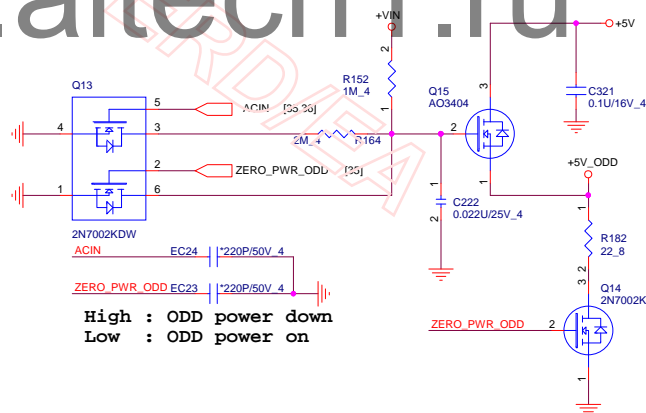
## 15" SATA ODD



<b>ODD CAP Setting</b>	C727/C728/C732/C732	C729/C730/C731/C733
<b>ODD 14"</b>	<b>O</b>	<b>X</b>
<b>ODD 15"/17"</b>	<b>X</b>	<b>O</b>

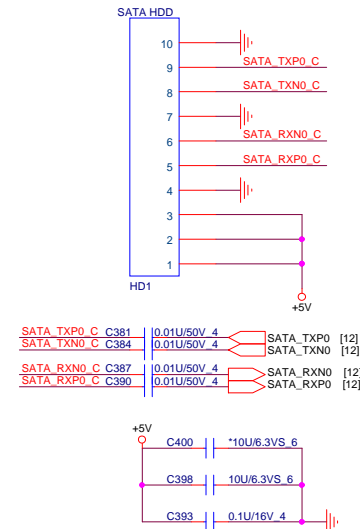
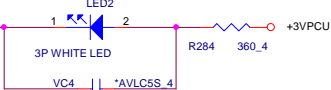


**SATA LED**



High : ODD power down  
Low : ODD power on

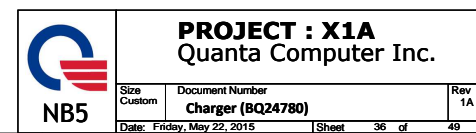
**PWR LED**

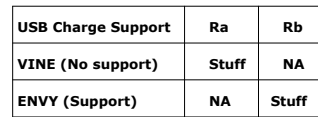


**PROJECT : X1A**  
Quanta Computer Inc.

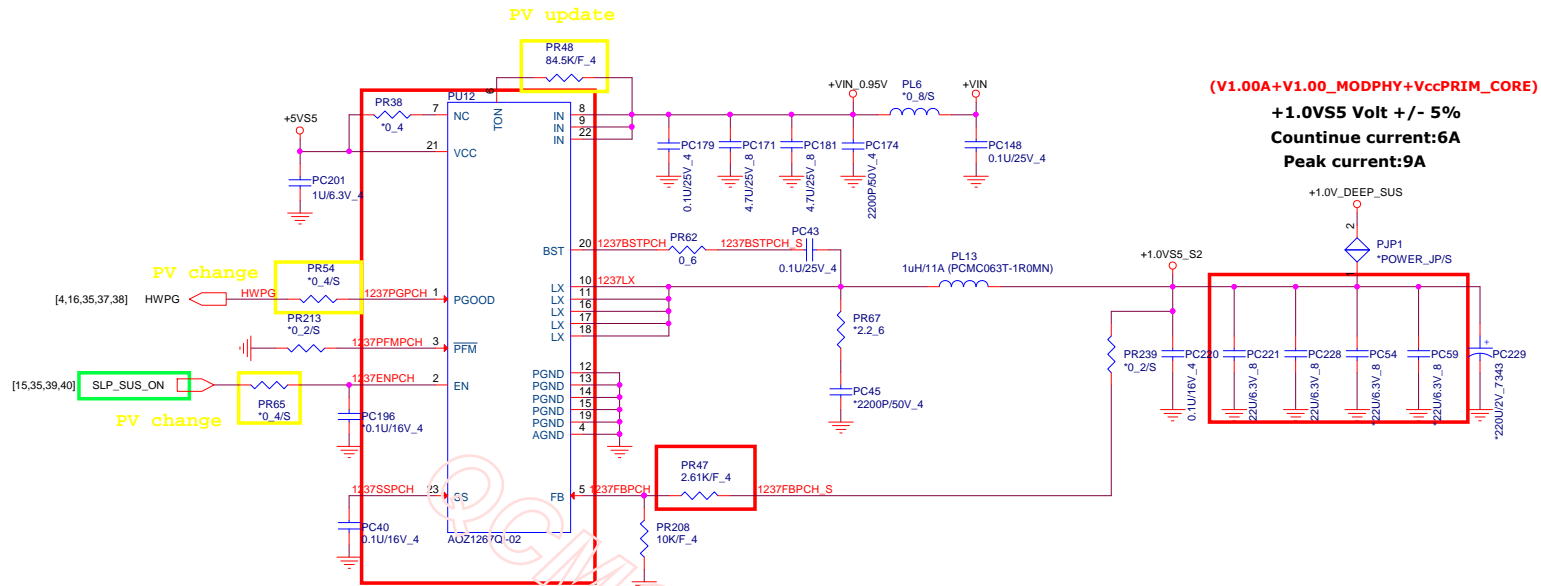
Size Custom	Document Number <b>WLAN/NGFF/MSATA</b>	Rev 1A
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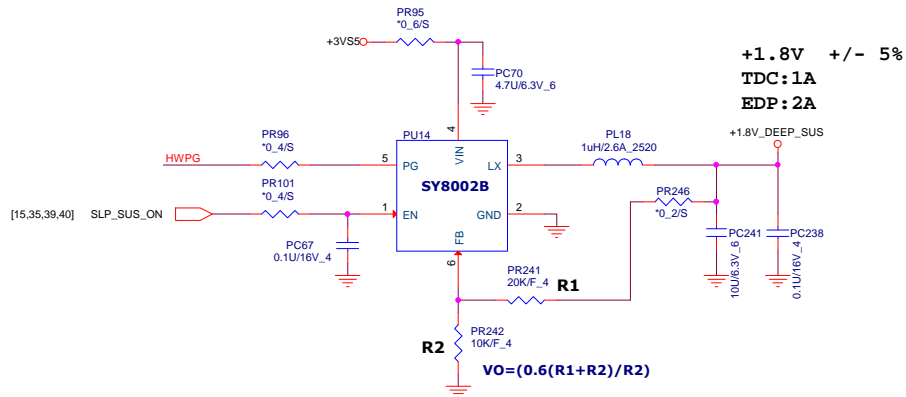








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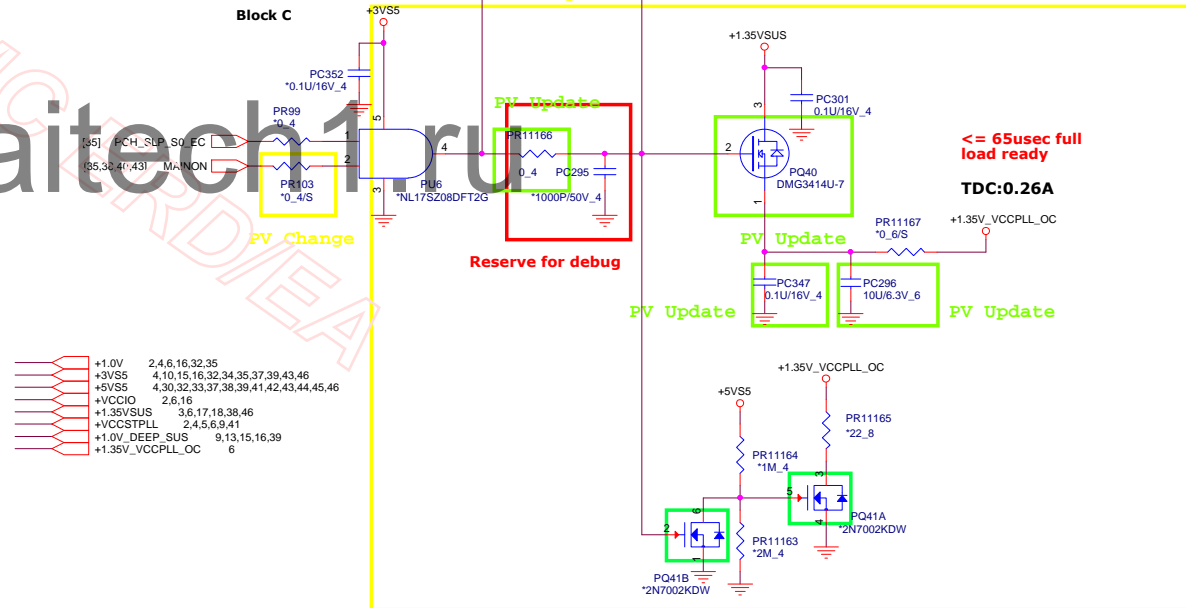
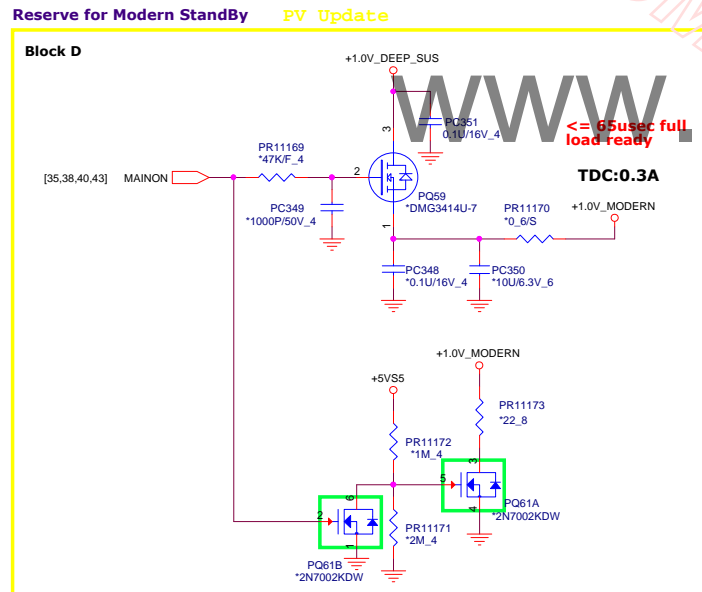
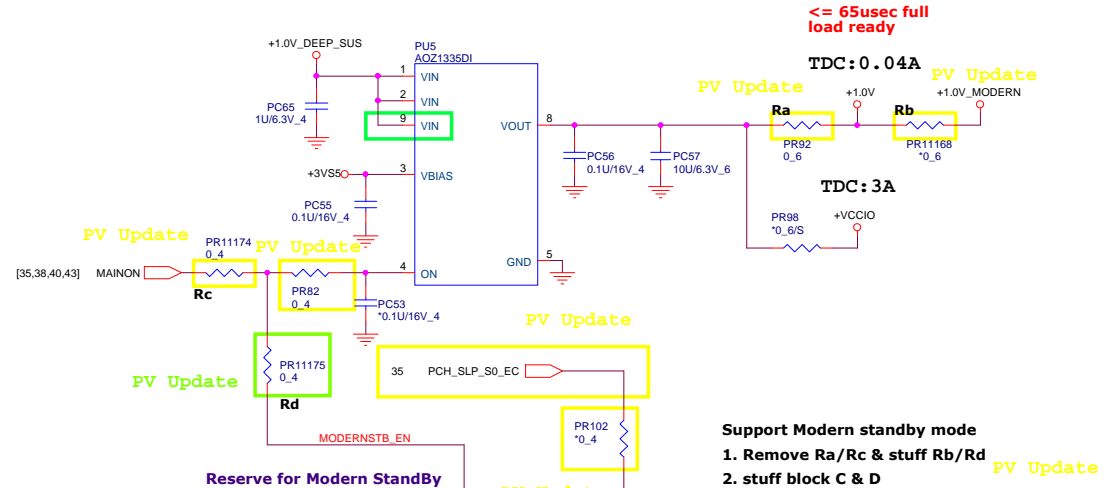
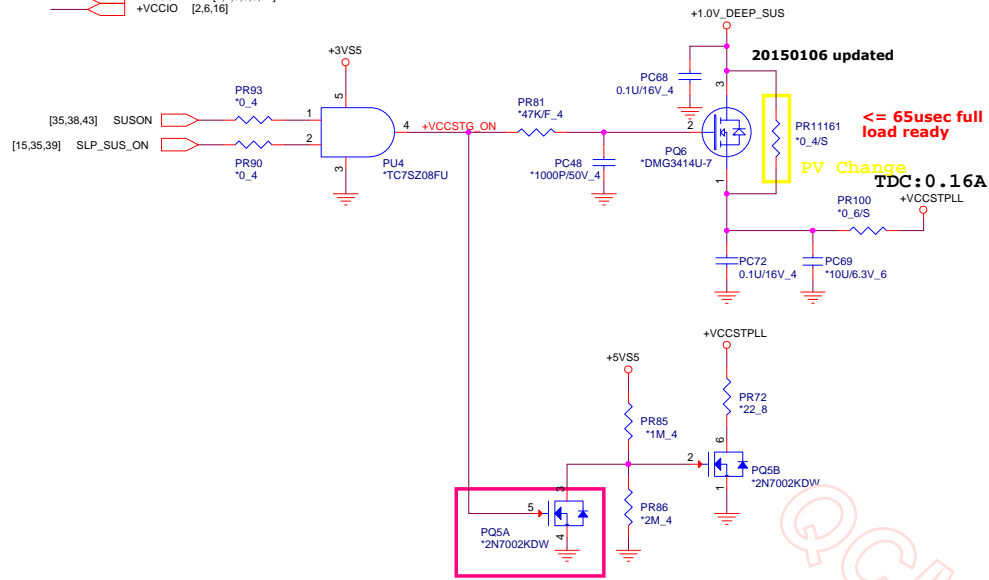


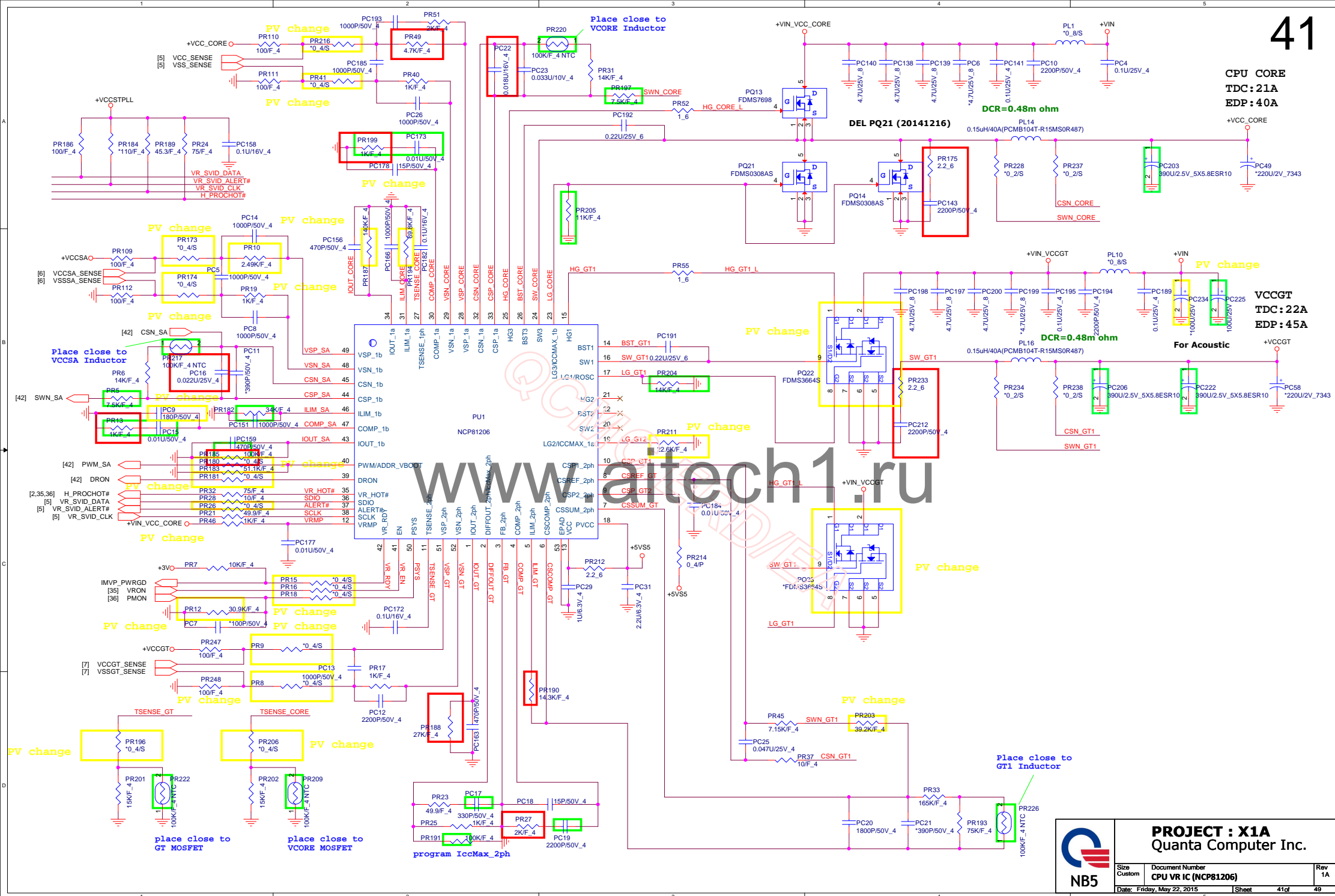
+VIN [28,31,33,34,36,37,38,41,42,43,44,45]  
 +3VS5 [4,10,15,16,32,34,35,37,40,43,44,46]  
 +5VS5 [4,30,32,33,37,38,40,41,42,43,44,46]

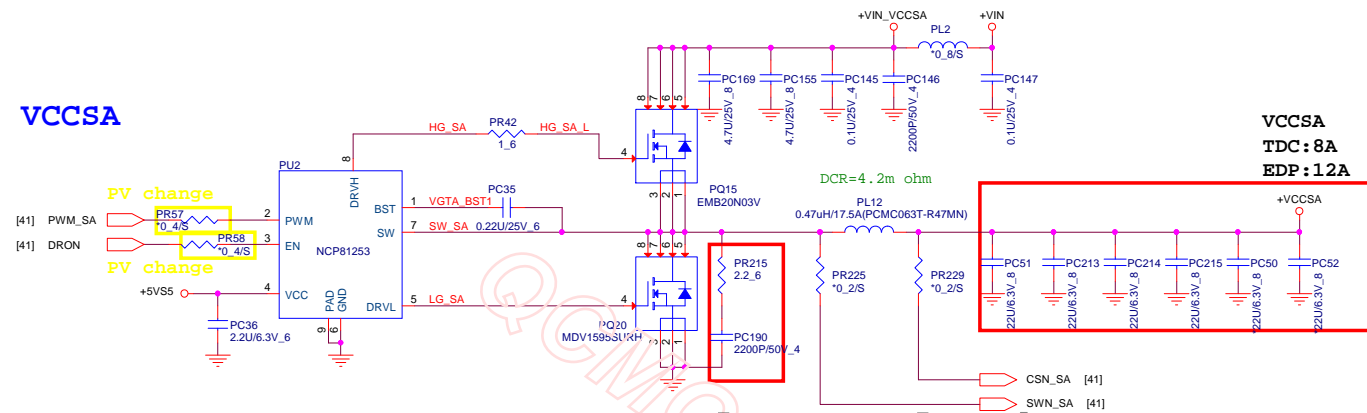


Diagram showing four input pins connected to a single internal node, with associated voltage levels and pin numbers:

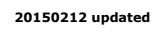
- +1.0V\_DEEP\_SUS [9,13,15,16,39]
- +1.0V [2,4,6,16,32,35]
- +3VS5 [4, 10,15,16,32,34,35,37,39,43,44,46]
- +VCCSTPLL [2,4,5,6,9,41]
- +VCCIO [2,6,16]



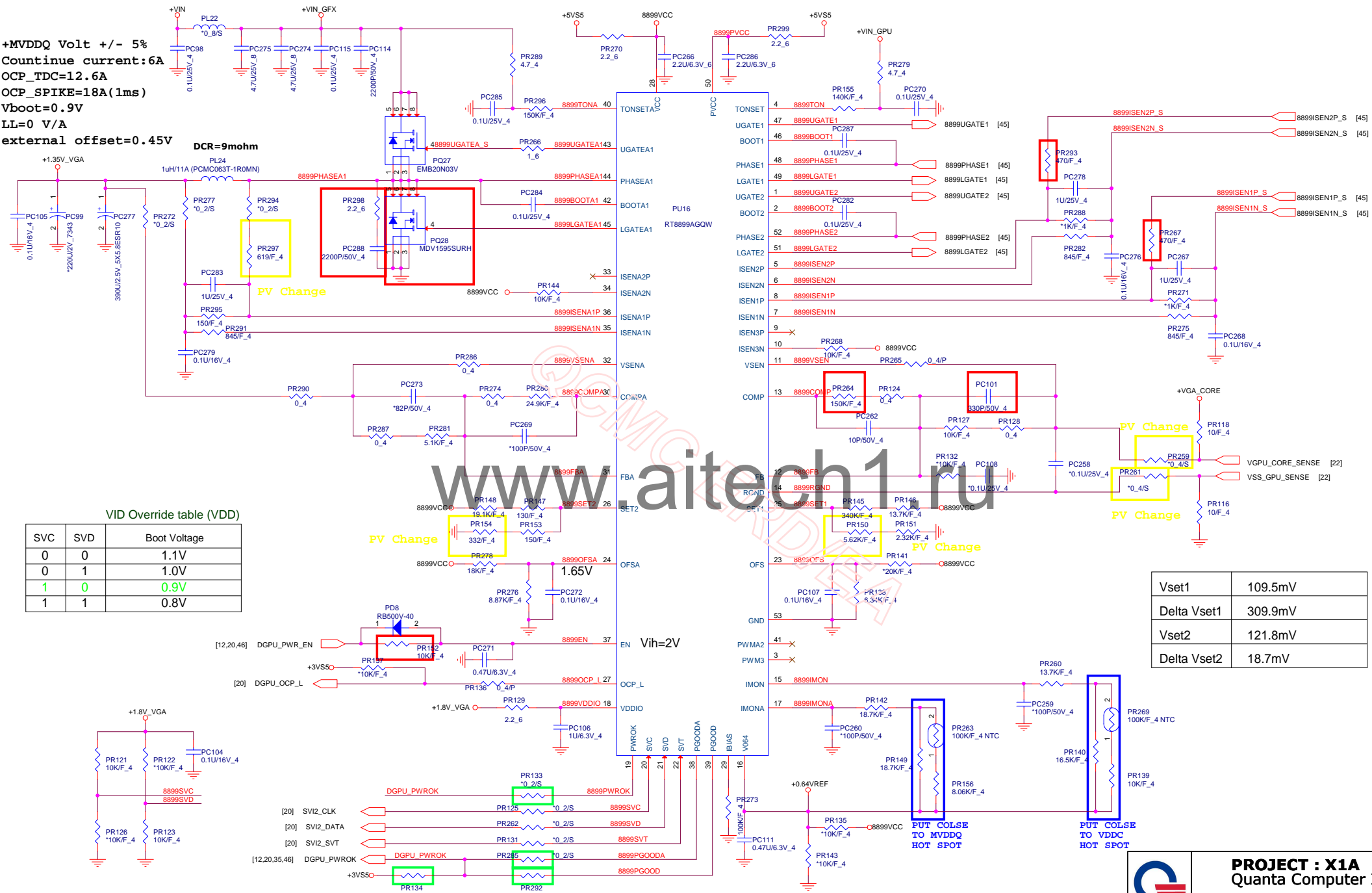




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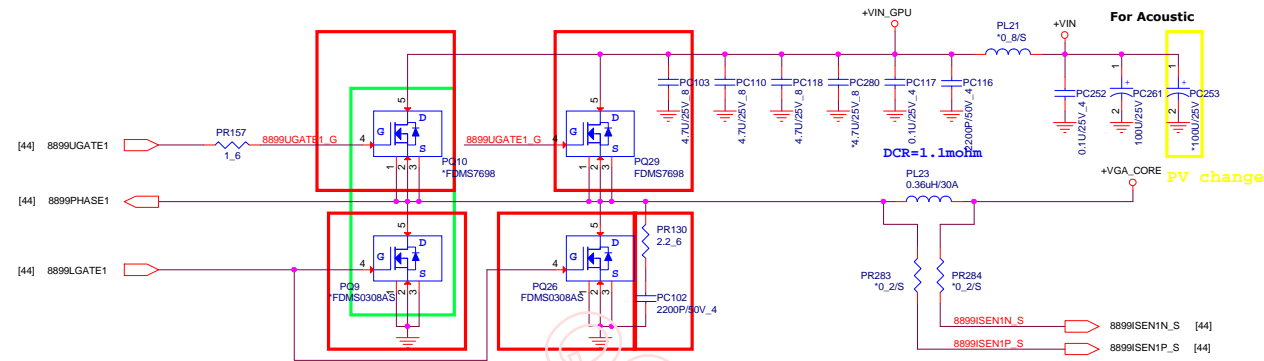


```
+MVDDQ Volt +/- 5%
Countinue current:6A
OCP_TDC=12.6A
OCP_SPIKE=18A(1ms)
Vboot=0.9V
LL=0 V/A
external offset=0.45V
```

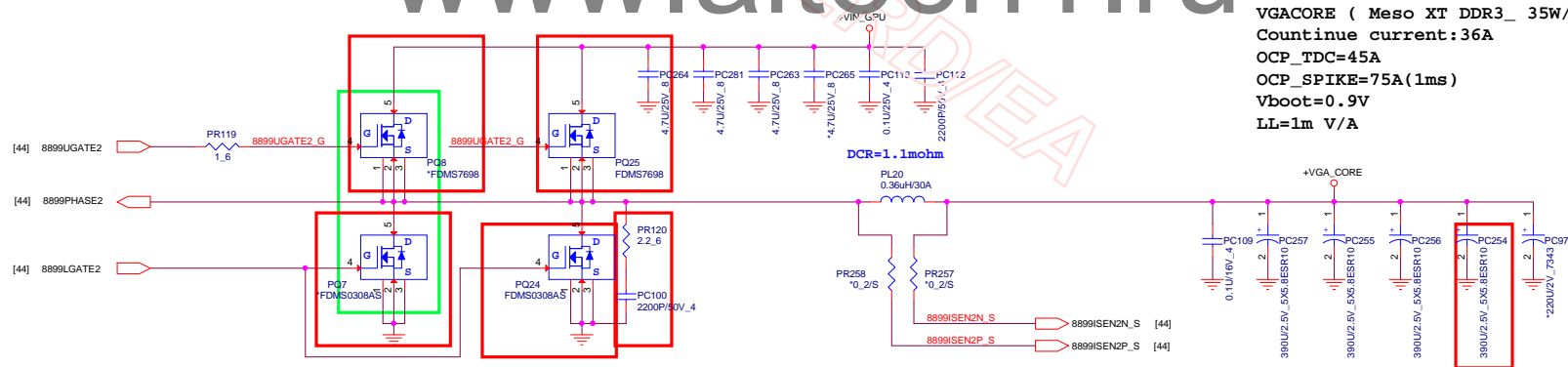


SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

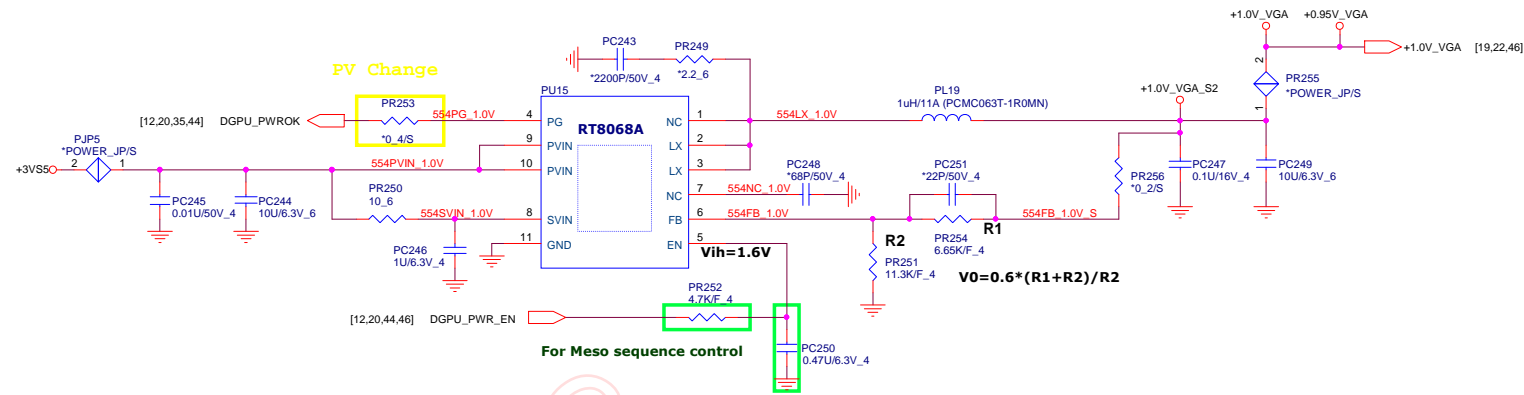
Vset1	109.5mV
Delta Vset1	309.9mV
Vset2	121.8mV
Delta Vset2	18.7mV



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VGACORE ( Meso XT DDR3\_ 35W/53W(1ms) )  
 Countinue current:36A  
 OCP\_TDC=45A  
 OCP\_SPIKE=75A(1ms)  
 Vboot=0.9V  
 LL=1m V/A



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